Supreme Court, U.S.
FILED

02 262 AUG 1 4 2002

OFFICE OF THE CLERK

No.

# In the Supreme Court of the United States

**TECHSEARCH, L.L.C.,**

*Petitioner,*

v.

**INTEL CORPORATION,**

*Respondent.*

**On Petition for Writ of Certiorari to the United States Court of Appeals for the Federal Circuit**

## APPENDIX TO PETITION FOR WRIT OF CERTIORARI

RAYMOND P. NIRO
*Counsel of Record*
JOHN C. JANKA
ROBERT P. GREENSPOON
NIRO, SCAVONE, HALLER & NIRO
181 West Madison Street
Suite 4600
Chicago, Illinois 60602
(312) 236-0733

*Attorneys for Petitioner TechSearch, L.L.C.*

Midwest Law Printing Company/Photex — Chicago — (312) 321-0220

107 pp

## TABLE OF CONTENTS

APPENDIX A: PAGE

Order, United States Court of Appeals for the Federal Circuit (Filed June 4, 2002) ..... 1

APPENDIX B:

Opinion, United States Court of Appeals for the Federal Circuit (Decided April 11, 2002) ..... 4

APPENDIX C:

Memorandum Decision and Order, United States District Court Northern District of California (Filed November 9, 1999) ..... 47

APPENDIX D:

Order, United States District Court Northern District of California (Filed February 3, 2000) ..... 67

APPENDIX E:

Order, United States District Court Northern District of California (Filed February 16, 2000) ..... 73

APPENDIX F:

Memorandum Decision and Order, United States District Court Northern District of California (Filed January 31, 2000) ..... 75

APPENDIX G:

Order, United States District Court Northern District of California (Filed December 16, 1999) ..... 95

APPENDIX H:

Order, United States District Court Northern District of California (Filed November 15, 1999) ..... 97

APPENDIX I:

Letter to District Court Judge from Intel's counsel (Dated August 1, 2000) ..... 99

APPENDIX J:

Letter to District Court Judge from Tech-Search's counsel (Dated August 2, 2000) ..... 102

**APPENDIX A**

**UNITED STATED COURT OF APPEALS**
**FOR THE FEDERAL CIRCUIT**

00-1226, -1250

**TECHSEARCH L.L.C.,**

Plaintiff-Appellant,

v.

**INTEL CORPORATION,**

Defendant-Cross Appellant.

**ORDER**

United States Court of Appeals for the Federal Circuit

ORDER

A combined petition for panel rehearing and for rehearing en banc having been filed by the APPELLANT, and a response thereto having been invited by the court and filed by the CROSS-APPELLANT, and the petition for rehearing having been referred to the panel that heard the appeal, and thereafter the petition for rehearing en banc and response having been referred to the circuit judges who are in regular active service,

UPON CONSIDERATION THEREOF, it is

ORDERED that the petition for panel rehearing be, and the same hereby is, DENIED and it is further

ORDERED that the petition for rehearing en banc be, and the same hereby is, DENIED.

The mandate of the court will issue on June 11, 2002.

Circuit Judge LINN did not participate in the vote

FOR THE COURT
/s/ Jan Horbaly (av)
Jan Horbaly
Clerk

Dated: June 4, 2002

cc: Raymond P. Niro
Matthew D. Powers

FILED JUN 4 - 2002
JAN HORBALY
CLERK

TECHSEARCH V INTEL CORP, 00-1226,-1250
(DCT -98-cv-3484)

**********

Note: Pursuant to Fed. Cir. R. 47.6, this order is not citable as precedent. It is a public record.

**********

**APPENDIX B**

TECHSEARCH L.L.C., Plaintiff-Appellant, v.
INTEL CORPORATION, Defendant-Cross Appellant.

00-1226, 00-1250

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

286 F.3d 1360; 2002 U.S. App. LEXIS 7202;
62 U.S.P.Q.2D(BNA) 1449

April 11, 2002, Decided

SUBSEQUENT HISTORY: [**1] Rehearing and Rehearing En Banc Denied June 4, 2002, Reported at: *2002 U.S. App. LEXIS 13552.*

PRIOR HISTORY: Appealed from: United States District Court for the Northern District of California. Senior Judge William H. Orrick.

DISPOSITION: AFFIRMED.

CASE SUMMARY

PROCEDURAL POSTURE: Plaintiff patent purchaser alleged that a line of defendant alleged infringer's microprocessors infringed the claims of its "927" patent. The United States District Court for the Northern District of California issued summary judgment of noninfringement and dismissed as moot the alleged infringer's counterclaims. The purchaser appealed.

OVERVIEW: This patent infringement case dealt with complex computer microprocessor technology. The patent was entitled "RISC Architecture Computer Configured for Emulation of the Instruction Set of a Target Computer."

The acronym RISC stood for "Reduced Instruction Set Computer." The patent disclosed a RISC architecture computer microprocessor that could emulate the architectural behavior of another microprocessor. The claimed RISC processor and emulation technique permitted use of existing software written for a target computer, even if that computer was a Complex Instruction Set Computer or "CISC" microprocessor, while retaining the benefits inherent in RISC processors. RISC architecture chips had having fewer gates, used less power, and executed instructions significantly faster than a typical CISC microprocessor. The appellate court's opinion focused on Claims 1, 4, and 14, the independent claims of the patent. It agreed with the claim construction articulated by the district court and concluded that the district court properly granted the alleged infringer's motion for summary judgment. It found that the district court did not abuse its discretion in the use of a technical advisor.

OUTCOME: The judgment was affirmed.

CORE TERMS: microprocessor, register, bit, advisor, target, patent, decoder, emulation, architecture, infringement, emulate, emulated, processor, native, summary judgment, indirect, redefine, emulating, multiplexer, microinstruction, safeguard, execute, arithmetic, plurality, appointment, width, noninfringement, corresponding, processed, configured

CORE CONCEPTS -

Patent Law: Infringement: Summary Judgment

Civil Procedure: Appeals: Standards of Review: Standards Generally

The appellate court reviews a district court's grant of summary judgment without deference. The moving party is entitled to summary judgment if the pleadings, depositions, answers to interrogatories, and admissions on file, together

with the affidavits, if any, show that there is no genuine issue as to any material fact and that the moving party is entitled to a judgment as a matter of law. Fed. R. Civ. P. 56(c). In reviewing the district court's grant of summary judgment, the appellate court draws all reasonable inferences from the evidence in favor of the non-movant. Summary judgment is appropriate when it is apparent that only one conclusion as to infringement could be reached by a reasonable jury. Summary judgment of noninfringement is also appropriate where the patent owner's proof is deficient in meeting an essential part of the legal standard for infringement, because such failure will render all other facts immaterial.

Patent Law: Infringement

Civil Procedure: Appeals: Standards of Review: Standards Generally

A patent infringement analysis involves two steps: (1) claim construction; and (2) application of the properly construed claim to the accused product. The first step, claim construction, is a matter of law that this court reviews without deference. Whether the accused device contains an element corresponding to each claim limitation or its equivalent is a question of fact, which, on summary judgment, is a question the appellate court reviews to determine whether a material factual issue remains genuinely in dispute.

Patent Law: Infringement: Summary Judgment

To support a summary judgment of noninfringement it must be shown that, on the correct claim construction, no reasonable jury could have found infringement on the undisputed facts or when all reasonable factual inferences are drawn in favor of the patentee. Similarly, although equivalence is a factual matter normally reserved for a factfinder, the trial court should grant summary judgment in any case where no reasonable factfinder could find equivalence.

Patent Law: Infringement: Claim Interpretation

An infringement analysis is a two-step process in which the court first determines the correct claim scope, and then compares the properly construed claim to the accused device to determine whether all of the claim limitations are present either literally or by a substantial equivalent. To establish literal infringement, all of the elements of the claim, as correctly construed, must be present in the accused system.

Civil Procedure: Summary Judgment: Supporting Papers & Affidavits

A party may not overcome a grant of summary judgment by merely offering conclusory statements.

Patent Law: Infringement

The mere recital of the mantra that the accused device performs the same function, in the same way, to achieve the same result, without more, does not create a genuine issue of material fact as to whether an accused device infringes by equivalents.

Patent Law: Infringement: Burdens of Proof

Patent infringement must be shown literally or equivalently for each limitation; general assertions of facts, general denials, and conclusory statements are insufficient to shoulder the non-movant's burden. Thus, the party opposing the motion for summary judgment of noninfringement must point to an evidentiary conflict created on the record, at least by a counter-statement of a fact set forth in detail in an affidavit by a knowledgeable affiant. Mere denials or conclusory statements are insufficient.

Civil Procedure: Summary Judgment: Burdens of Production & Proof

Unsupported or conclusory averments are insufficient to avoid summary judgment where the moving party has met its initial burden.

Patent Law: Infringement: Summary Judgment

The motion of an accused infringer for judgment on the ground of non-infringement of a patent may be granted where the patentee's proof is deficient in meeting an essential part of the legal standard for infringement. The court has further recognized that specific claim limitations cannot be ignored as insignificant or immaterial in determining infringement.

Civil Procedure: Appeals: Standards of Review: Abuse of Discretion

Evidence: Procedural Considerations

Procedural rulings are reviewed by the appellate court under regional circuit law, unless the procedural issues are unique to patent law. Further, the appellate court applies regional circuit law to procedural issues that are not themselves substantive patent law issues. The use of a technical advisor to assist the district court in understanding complex scientific and technical factual issues, is not limited to and unique to patent cases. Technical advisors may be useful for the understanding of scientific evidence generally as well as the science or technology involved in patent cases. Because understanding issues of complex science and technology is not so unique as to clearly implicate the jurisdictional responsibilities of the appellate court in a field within its exclusive jurisdiction, it applies regional procedural law. The United States Court of Appeals for the Ninth Circuit applies the abuse of discretion standard to a district court's appointment of a technical advisor.

Evidence: Procedural Considerations

A technical advisor is helpful in assisting the court in understanding the scientific and technical evidence it must consider. Such evidence in a patent case includes expert testimony, scientific articles and texts, and patents, upon which the court must rely in understanding the technology so that it can interpret the patent claims and determine whether to grant motions for summary judgment of validity, invalidity, infringement or noninfringement, and to assist the court in articulating appropriate jury instructions.

Evidence: Procedural Considerations

The district court is the gatekeeper of the trial in determining when scientific evidence is properly admissible. Because this function is critical, the district court must have the authority to appoint a technical advisor in such instances so that the court can better understand scientific and technical evidence in order to properly discharge its gatekeeper role of determining the admissibility of such evidence. However, the federal courts of appeals must determine, the extent, if any, to which a district court has established safeguards to prevent the technical advisor from introducing new evidence and to assure that the technical advisor does not influence the district court's review of the factual disputes.

Evidence: Procedural Considerations

The law has long recognized that it may effectively use the knowledge of experts to inform and support the judicial process to settle disputes. The United States Supreme Court has noted that courts have, at least in the absence of legislation to the contrary, inherent power to provide themselves with appropriate instruments required for the performance of their duties. This power includes authority to appoint persons unconnected with the court to aid judges in the performance of specific judicial duties, as they may arise in the progress of a cause.

Evidence: Procedural Considerations

The trial court's inherent search for truth is the basic building block by which the judicial process maintains its credibility within the fabric of our society. In this search, it cannot be expected that trial judges will have expertise in biotechnology, microprocessor technology, organic chemistry, or other complex scientific disciplines. Therefore, in those limited cases where the scientific complexity of the technology is such that the district court may require the assistance of a technical advisor to aid in understanding the complex technology underlying the patent, it has the inherent authority to appoint such an advisor.

Civil Procedure: Appeals: Standards of Review: Abuse of Discretion

Evidence: Witnesses: Court-Appointed Experts

A district court's appointment of a technical advisor, outside of the purview of Fed. R. Evid. 706, falls within the district court's inherent authority, and the United States Court of Appeals for the Ninth Circuit has held that district courts may use technical advisors when desirable and necessary. It also implicitly recognized that district courts should use this inherent authority sparingly and then only in exceptionally technically complicated cases. Therefore, the United States Court of Appeals for the Federal Circuit applies the law of the regional circuit and reviews the appointment of the technical advisor, and whether the district court properly followed appropriate procedural safeguards, for abuse of discretion.

Civil Procedure: Appeals: Standards of Review: Standards Generally

Although the United States Court of Appeals for the Ninth Circuit has recognized the need for district courts to avoid impropriety, it has not held precisely what procedural safeguards district courts should employ. Thus, to establish

a basis for appellate review, if the regional circuit court has not specifically spoken on the issue, the court must reasonably predict how that court would decide the issue.

Evidence: Procedural Considerations

The district court in appointing a technical advisor must: use a fair and open procedure for appointing a neutral technical advisor, addressing any allegations of bias, partiality or lack of qualifications in the candidates; clearly define and limit the technical advisor's duties, presumably in a writing disclosed to all parties; guard against extra-record information; and make explicit, perhaps through a report or record, the nature and content of the technical advisor's tutelage concerning the technology. The fact that the use of a technical advisor is permissible under such guidelines does not mean that it is invariably desirable or that safeguards are not required. As a practical matter, there is a risk that some of the judicial decision-making function will be delegated to the technical advisor. District court judges need to be extremely sensitive to this risk and minimize the potential for its occurrence.

Evidence: Witnesses: Court-Appointed Experts

Unlike a technical advisor, an expert witness appointed by the court may be relied upon as a source of evidence and may be called upon to testify.

COUNSEL: John C. Janka, Niro, Scavone, Haller & Niro, of Chicago, Illinois, argued for plaintiff-appellant. With him on the brief were Raymond P. Niro, and Robert P. Greenspoon. Of counsel was Joseph N. Hosteny.

Matthew D. Powers, Weil, Gotshal & Manges LLP, of Menlo Park, California, argued for defendant-cross appellant. With him on the brief was Edward R. Reines. Of counsel were Josh A. Krevitt, and Elizabeth B. Honkonen.

JUDGES: Before NEWMAN, GAJARSA, and DYK, Circuit Judges. Opinion for the court filed by Circuit Judge GAJARSA. Concurring opinion filed by Circuit Judge Dyk.

OPINION BY: GAJARSA

OPINION:

[*1363] GAJARSA, Circuit Judge.

This is a patent infringement case dealing with complex computer microprocessor technology. After extensive submissions by the parties and numerous preliminary findings by the United States District Court for the Northern District of California, the court issued summary judgment of noninfringement of TechSearch's U.S. Pat. No. *5,574,927* ("the *'927* patent"), issued to Henry L. Scantlin, in favor of Intel Corp. ("Intel") and dismissed as [**2]moot Intel's counterclaim for declaratory relief. TechSearch, L.L.C. v. Intel Corp., No. 98-CV-03484, slip op. at 17-18 (N.D. Cal. January 31, 2000) (memorandum decision and order granting summary judgment) ("TechSearch-Judgment"). TechSearch L.L.C. ("TechSearch") appeals from the grant of summary judgment. For the reasons discussed below, we affirm the judgment of the district court.

BACKGROUND

In the early 1990's, International Meta Systems, Inc. ("IMS") sought to develop a microprocessor known as the "IMS 3250" that could "emulate," or behave like, popular microprocessors such as the Intel 80X86 and the Motorola 680X0. On March 25, 1994, IMS filed a patent application encompassing the IMS 3250 processor. The application issued as the *'927* patent on November 12, 1996. The inventor, Henry L. Scantlin, assigned all rights in the *'927* patent to IMS, his employer.

The patent is entitled "RISC Architecture Computer Configured for Emulation of the Instruction Set of a Target

Computer." The acronym RISC stands for "Reduced Instruction Set Computer." The patent discloses a RISC architecture computer microprocessor that can emulate the architectural behavior of another microprocessor.[**3] The claimed RISC processor and emulation technique permit use of existing software written for a target computer, even if that computer is a Complex Instruction Set Computer or "CISC" microprocessor, while retaining the benefits inherent in RISC processors. *'927* patent, col. 2, ll. 52-57.

CISC architecture requires an extensive fixed set of, as the name suggests, complex instructions that are either hardwired or microprogrammed into the logic of a single microprocessor. *'927* patent, col. 1, ll. 54-60. A RISC architecture design has certain design benefits compared to CISC microprocessor designs because a RISC architecture reduces the complexity of the chip through the use of microinstructions that perform a limited subfunction of a CISC instruction within a single clock cycle. *'927* patent, col. 1, ll. 60-68. Thus, RISC architecture results in a microprocessor chip having fewer gates, using less power, and executing instructions significantly faster than a typical CISC microprocessor. *'927* patent, col. 2, ll. 1-11.

Claims 1, 4 and 14 are the independent claims of the *'927* patent, and read as follows:

1. A method for emulating the instruction set of a target computer on a RISC [**4]architecture computer, comprising the steps of:

1) fetching a target instruction of a format compatible with the instruction set of the target computer;

2) parsing and decoding said instruction into fields designating an opcode and operands;

3) converting said opcode into an address pointing to a sequence of one or more microcoded instructions;

[*1364] 4) decoding said microcoded instruction into a LHS instruction having fields essentially compatible with a RISC architecture and a RHS instruction having fields to select a plurality of indirect registers pointing to emulated registers;

5) processing said emulated registers with an arithmetic logic unit;

6) calculating a condition code as a function of the operation of said arithmetic logic unit and a selection field within said microcoded instruction;

7) storing a result of said processing by said arithmetic logic unit;

8) storing a result of said condition code calculation; and

9) repeating steps 4-8 with a next microcoded instruction until an end of said microcoded sequence is encountered and then continuing at step 1 with a next target instruction.

*'927* patent, col. 52, l. 64 to col. 53, l. 23.

4. A RISC architecture computer[**5] having a native instruction width of N bits configured for emulating target instructions from the instruction set of a target computer, comprising:

a plurality of emulation registers capable of corresponding to registers in the target computer and having data widths greater than or equal to the data widths of the registers in the target computer;

a plurality of indirect registers for selection of said emulation registers; parsing means to extract a plurality of data fields from a target instruction, at least one said fields including an opcode;

dispatching means using said opcode to direct the RISC architecture computer to select at least one M+N bit expanded RISC instruction from a microcode memory;

an expanded instruction decoder for using said M bits from each said expanded RISC instruction to redefine the RISC architecture computer in terms of the target computer, wherein said M bits define fields, said fields comprising a width field for designating the data width of said emulation registers and the data width of an arithmetic function, an indirect register field for designating said indirect registers, and a condition code field for designating a condition code emulation[**6] mode; and

condition code calculation means for determining the condition code for an arithmetic function according to said condition code field.

*'927* patent, col. 53, ll. 33-61.

14. A RISC architecture computer having a native instruction width of N bits configured for emulating target instructions from the instruction set of a target computer, comprising:

a plurality of emulation registers capable of corresponding to registers in the target computer and having data widths greater than or equal to the data widths of the registers in the target computer;

a plurality of indirect registers for selection of said emulation registers; parsing means to extract a plurality of data fields from a target instruction, at least one said field including an opcode;

[*1365] dispatching means using said opcode to direct the RISC architecture computer to select at least one M+N bit expanded RISC instruction from a microcode memory;

an expanded instruction decoder for using said M bits from each said expanded RISC instruction to redefine the

RISC architecture computer in terms of the target computer; and condition code calculation means for determining the

condition code for an arithmetic[**7] function in accordance with the target computer.

*'927* patent, col. 54, ll. 19-43.

As claimed, the invention includes a system or method for using a RISC architecture computer having a native instruction set including, inter alia, instructions of a width of N bits configured for emulating instructions from the instruction set of a target computer; a plurality of emulation registers for simulating registers of the target computer; a plurality of indirect registers for selecting the emulation registers; structure for extracting the data fields of a target instruction, including an opcode field; structure for using the opcode to direct the RISC architecture computer to select at least one M+N bit expanded RISC instruction from memory; an expanded instruction decoder for using M bits from the expanded RISC instruction to redefine the RISC architecture computer in terms of the target computer; a condition code field for designating a condition code emulation mode; and structure for determining the condition code for an arithmetic function according to a condition code field.

Intel's x86 CISC microprocessors share instructions, adding new instructions to those which comprise[**8] the instruction set of the previously issued microprocessor. In other words, with the introduction of each new member of the Intel x86 family of microprocessors, new instructions are added to the CISC x86 instruction set of the previous version of the microprocessors. Thus, the P6 instruction set includes instructions unique to that version of the processors, as well as those used by the P5 microprocessor. Like the P6, the P5 instruction set includes all of the instructions found in the instruction set of the 486 microprocessor,

as well as each additional instruction unique to the P5. Thus, each new processor executes all of the instructions of its predecessor, without modification, as well as the new instructions unique to that device.

After working on several versions of the 3250, IMS's attempts to produce the microprocessor commercially failed. TechSearch purchased the '927 patent as an asset in the IMS bankruptcy proceeding. Subsequently, TechSearch filed a complaint against Intel in September 1998 alleging that Intel's P6 line of microprocessors infringed the claims of the '927 patent.

The district court held a Markman hearing in August 1999 and issued a Memorandum Decision[**9] and Order on November 1, 1999. Recognizing that one skilled in the art would typically identify a computer as RISC- or CISC-based upon its published instructions rather than the microinstructions, the court concluded that, in the context of the patented invention, the classification of the microprocessor was properly assessed from the microcode level. The court concluded that the claims themselves confirm that it is the microcode, not the machine code (or "macro" level), that is relevant to whether a microprocessor is a [*1366] CISC or RISC microprocessor, and is therefore covered by the patent's claims.

With regard to the term "emulation," the district court referenced the written description that defines the term as "a process in which one computer X behaves identically to another computer Y, as X executes the instructions of Y, where the internal architectures of computers X and Y are different." '927 patent, col. 2, ll. 30-33. Concerning the "LHS" (left-hand side) and "RHS" (right-hand side) of the coded instruction recited in claim 1, the court determined that those terms refer to the native instruction of a RISC microprocessor configured for emulation of a target computer's microprocessor. [**10]Thus, the court concluded

that the LHS and RHS are two subdivisions of a single RISC microinstruction.

Independent claims 4 and 14 refer to the coded instruction as an M+N bit expanded RISC instruction. The court concluded that the M+N bit expanded RISC instruction is composed of N bits corresponding to the native instruction, or the instruction of the host microprocessor's instruction set used when the microprocessor is not in emulation mode, and M bits "which redefines the N bits" in the expanded RISC instruction, thereby enabling the host microprocessor to emulate a target computer.

The district court defined the term "condition code" as a summary of the effects of recently emulated target instructions. Although worded differently, the district court noted that the parties agreed that each independent claim requires a selection field within the microinstruction identifying the particular target computer being emulated so that the condition code matches the operation that would have been performed had the same calculation been performed within the target computer. Finally, the district court interpreted the "expanded instruction decoder" as simply a decoder used in the execution [**11]of an M+N bit RISC instruction.

Subsequently, the parties filed cross-motions for summary judgment. On January 31, 2000, the district court issued a Memorandum Decision and Order granting Intel's motion for summary judgment of noninfringement. The district court concluded that to prove infringement of claim 1, TechSearch must show that the P6 microprocessors have "a plurality of indirect registers pointing to emulated registers," and that the accused products process the emulated registers with an arithmetic logic unit. TechSearch had maintained that the macro alias register file ("MAR") found in the P6 corresponds to the claimed indirect registers. The court determined that, even assuming that to be

true, there is no dispute that the MAR does not point to emulated registers as required and that there are no registers in the P6 that are both pointed to by the indirect registers and processed with an arithmetic logic unit ("ALU"). Specifically, the court noted that the MAR does not point to any registers or to anything processed by the ALU and that the MAR are logical registers, which are not actual registers but merely references. Nor was the court persuaded that TechSearch had established[**12] that there are any emulated registers in the accused device. Therefore, the court determined that claim 1 is not infringed literally or under the doctrine of equivalents.

The court further concluded that the P6 microprocessors are not "configured to emulate the instruction set of a target computer" in accordance with claims 1, 4 and 14. The district court found that "it is beyond dispute that the P6 microprocessors [*1367] are not configured to emulate in the manner claimed," TechSearch-Judgment, slip op. at 9, and therefore do no infringe. The court noted that "the 'patent specification makes clear that its emulation scheme entails modifying preexisting native instructions of a RISC architecture computer'" such that when the computer is emulating, "the native instructions are redefined by M bits in order to form an M+N bit expanded instruction that enables the host system to emulate the target system." Id. at 9-10. Accordingly, the court determined that to infringe claims 4 and 14, TechSearch must prove that the P6 microprocessor has both a native instruction of N bits and an expanded RISC instruction comprised of M+N bits to be used when the computer is emulating, or their equivalents. [**13]

The court determined that no reasonable jury could find that the P6 microprocessors have microinstructions comprised only of N bit instructions when operating in the native mode of the host processor, i.e., when not emulating, and microinstructions comprised of an M+N bit RISC

instruction when emulating. The court noted that the format of the instructions that the P6 microprocessors use when executing an instruction from an "earlier version" of Intel's x86 instruction set are indistinguishable from the format of the instructions originating with the "current version." The court concluded that even were the testimony of TechSearch's expert to be accepted, asserting that the P6 microprocessors emulate, TechSearch has not shown infringement because it is "beyond question" that the P6 runs only one instruction set. Therefore, the court concluded that the P6 microprocessor does not emulate in the manner required by claims 4 and 14.

The district court further determined, in the alternative, that the P6 products do not have an "expanded instruction decoder" using M bits from each expanded RISC instruction to "redefine" the RISC architecture computer in terms of the target computer[**14] during emulation. Thus, the court concluded that it is "beyond cavil" that the P6 microprocessor does not infringe.

The court stated that to prove infringement of claims 4 and 14 TechSearch must prove that: (1) the P6 microprocessor has an expanded instruction decoder; and (2) that the expanded instruction decoder uses M bits from each expanded RISC instruction to "redefine" the RISC architecture computer in terms of the target computer during emulation. The district court concluded that the P6 microprocessor does not have a decoder that can decode expanded instructions.

The court concluded that the P6 "alias multiplexer," alleged by TechSearch to correspond to the claimed decoder, differs materially from the decoder contemplated by the patent. Specifically, the court noted that the claimed invention translates the instructions into a form for processing by the ALU in a manner involving considerable interaction between the various elements of the microinstruction.

Contrarily, the inputs of the multiplexer are simply routed to its outputs. The court noted that one of ordinary skill in the art would know that decoders and multiplexers perform substantially different functions and [**15]consist of substantially different structure.

The court noted that TechSearch's expert, Dr. Hoevel, did not contend that the multiplexer in the P6 microprocessor operates as a decoder and did not dispute that the function of multiplexing differs from the decoding claimed. While the court concluded that the claimed decoder combines the input signals to produce outputs [*1368] that cause selection of the direct, indirect or emulation registers, it found that TechSearch did not dispute that the P6 microprocessor's alias multiplexer architecture does not combine input signals, but simply steers each signal to the appropriate output field. The court, therefore, found Dr. Hoevel's testimony, and TechSearch's arguments based thereon, insufficient to avoid a grant of summary judgment of noninfringment.

Similarly, the court determined that TechSearch had failed to create a triable issue of fact by arguing that a multiplexer is capable of acting as a decoder, noting that TechSearch failed to provide evidence to explain how the multiplexer of the P6 functions in the manner describing the claimed decoder. The district court further concluded that Hoevel's conclusory allegations failed to raise a genuine[**16] issue of material fact.

Finally, noting that the claimed instruction decoder operates to "redefine" the microprocessor when emulating and that no redefinition of instructions is performed by the "decoder" in the P6 microprocessor, the court concluded that no part of the P6 can be found to infringe the instruction decoder recited in claims 4 and 14. Specifically, the court concluded that the P6 microprocessor does not use an additional M bits to redefine N bits of the instruction when

"emulating." Although Hoevel asserted that the microinstructions found in P6 microprocessors, known as "Cuops," contain fields for performing register indirection, the court noted that in the P6 microprocessors those instructions are always the same size and use all of its bits, regardless of the version of microprocessor with which they were first introduced. Thus, the court determined that the Cuops microinstruction, and thus the P6 microprocessor instruction set, does not redefine or expand the microinstructions as claimed. Therefore, the court concluded that no reasonable jury could find that the Cuops are redefined "in any way."

In a Memorandum Decision and Order dated November 9, 1999, issued[**17] after the Markman hearing but before the grant of summary judgment, the district court informed the parties that it had decided to appoint its own "technical advisor." The court recognized that such appointments should be reserved for the exceptional case, but deemed it appropriate in this particular case because infringement would be "a highly technical [issue] far beyond the boundaries of the normal questions of fact and law with which judges routinely grapple." The court noted that technical advisors "are not witnesses, and may not contribute evidence." As such, the court concluded that a technical advisor is not subject to the requirements set forth in Rule 706 of the Federal Rules of Evidence regulating the appointment of expert witnesses. The district court further explained that "[a] judge may not appoint a technical advisor to brief him on legal issues, or to find facts outside the record of the case; the advisor's role is to acquaint the judge with the jargon and theory disclosed by the testimony and to help think through certain of the critical technical problems." TechSearch, L.L.C. v. Intel Corp., No. 98-CV-03484, slip op. at 4 (N.D. Cal. November 9, 1999) (memorandum[**18] decision and order appointing technical advisor) ("TechSearch-Appointment"). Anticipating the diffi-

culty in evaluating the "extremely complicated" technical evidence submitted by the parties involving "highly technical electrical engineering and microprocessor design," which the district court had to process to formulate its claim construction, the court retained the technical [*1369] advisor to assist with evaluation of the technical matters before it when resolving pretrial motions, as well as during trial. Specifically, the court recognized that it would be "faced with expert testimony, scientific articles, and patents" the technology of which the court "urgently required" the assistance of a technical advisor to understand. As an example, the court stated that evaluation of the prior art required consideration of technical concepts beyond normal questions of fact regularly addressed by the court.

The court determined that its technical expert, Dr. Hearn, was a neutral third party, and explained its reasoning for that determination in its memorandum decision. TechSearch-Appointment, slip op. at 5-7. The court reiterated that Dr. Hearn had "agreed that he will not engage in any[**19] independent investigation of the underlying litigation, provide evidence to the Court, or contact any party or witness in this action." The court further agreed to identify any material relied upon by Dr. Hearn, other than that submitted by the parties or "those upon which a person versed in the relevant field of knowledge would be reasonably expected to rely." The court stated that Dr. Hearn would execute an affidavit indicating his understanding of that order before beginning his engagement, and would file an affidavit attesting to his compliance with its terms at the conclusion of his employment.

TechSearch appeals the district court's judgment. We have jurisdiction pursuant to *28 U.S.C. § 1295*(a)(1).

## STANDARD OF REVIEW

This court reviews a district court's grant of summary judgment without deference. *Cortland Line Co. v. Orvis Co.*,

*203 F.3d 1351, 1355, 53 USPQ2d 1734, 1746 (Fed. Cir. 2000).* The moving party is entitled to summary judgment "if the pleadings, depositions, answers to interrogatories, and admissions on file, together with the affidavits, if any, show that there is no genuine issue as to any material fact and that the[**20] moving party is entitled to a judgment as a matter of law." Fed. R. Civ. P. 56(c). In reviewing the district court's grant of summary judgment, this court draws all reasonable inferences from the evidence in favor of the non-movant. *Anderson v. Liberty Lobby, Inc., 477 U.S. 242, 255, 91 L. Ed. 2d 202, 106 S. Ct. 2505 (1986).* Summary judgment is appropriate when it is apparent that only one conclusion as to infringement could be reached by a reasonable jury. *ATD Corp. v. Lydall, Inc., 159 F.3d 534, 540, 48 USPQ2d 1321, 1324 (Fed. Cir. 1998).* Summary judgment of noninfringement is also appropriate where the patent owner's proof is deficient in meeting an essential part of the legal standard for infringement, because such failure will render all other facts immaterial. *London v. Carson Pirie Scott & Co., 946 F.2d 1534, 1537, 20 USPQ2d 1456, 1458 (Fed. Cir. 1991).*

A patent infringement analysis involves two steps: 1) claim construction; and 2) application of the properly construed claim to the accused product. *Markman v. Westview Instruments, Inc., 52 F.3d 967, 976, 34 USPQ2d 1321, 1326 (Fed. Cir. 1995)* (en banc[**21] ), aff'd, *517 U.S. 370, 134 L. Ed. 2d 577, 116 S. Ct. 1384 (1996).* The first step, claim construction, is a matter of law that this court reviews without deference. *Cybor Corp. v. FAS Tech., Inc., 138 F.3d 1448, 1454, 46 USPQ2d 1169, 1172 (Fed. Cir. 1998)* (en banc). Whether the accused device contains an element corresponding to each [*1370] claim limitation or its equivalent is a question of fact, which, on summary judgment, is a question we review to determine whether a material factual issue remains genuinely in dispute. *Roton Barrier,*

*Inc. v. Stanley Works, 79 F.3d 1112, 1125, 37 USPQ2d 1816, 1826 (Fed. Cir. 1996).*

DISCUSSION

I. Claim Construction

While the parties dispute the court's construction of many of the claim terms at issue before the district court, we address the construction of only those terms essential for disposition of this appeal.

The independent claims of the '927 patent recite a method or computer for "emulating" target instructions of the instruction set of a target computer using, inter alia, "emulation registers" capable of corresponding to registers in the target computer. The written description[**22] defines the term "emulation" generally as "a process in which one computer X behaves identically to another computer Y, as X executes the instructions of Y, where the internal architectures of computers X and Y are different." '927 patent, col. 2, ll. 30-33. We adopt this construction and conclude that the district court correctly interpreted this term.

Claims 4 and 14 define the particular manner in which the claimed processor emulates. Specifically, both claims require a "M+N bit expanded RISC instruction" with N bits defining the "native instruction . . . configured for emulating target instructions from the instruction set of a target computer." Consistently, the claims require an expanded instruction decoder that uses "M bits from each said expanded RISC instruction to redefine the RISC architecture computer in terms of the target computer." The written description of the '927 patent defines N bits of an expanded RISC instruction, also referred to as the LHS (left-hand side) of the instruction, as the number of bits of the instruction that the microprocessor uses "in its native mode." '927 patent, col. 5, ll. 1-2. With regard to the M bits of the

expanded RISC instruction, also [**23]referred to as the RHS (right-hand side) of the instruction, the *'927* patent states that "contained within the additional M bits [of the expanded RISC instruction] and used in conjunction with the N bits are directions on the use of resources within the RISC computer, peculiar to each emulated instruction." *'927* patent, col. 5, ll. 6-9. The written description of the *'927* patent explains that the M bits, or RHS, of the expanded RISC instruction are used "to redefine, during emulation of a target processor operation, the register data paths . . . of the LHS [or N bits of the expanded RISC instruction] to correspond to the target processor instruction being emulated, permitting the host processor to mirror, without physical changes, the target processor architecture being emulated." *'927* patent, col. 8, ll. 31-37. Consistently, TechSearch's expert, Dr. Hoevel, recognizes that to emulate, "the host computer has to interpret and execute the target instruction set used in the target computer . . . and claims 1 through 3 of the *'927* patent reveal the advantages of the special kind of emulation and backwards compatibility found in the *'927* patent."

We conclude, as the district court[**24] did, that the M+N bit expanded RISC instruction recited in claims 4 and 14 includes N bits corresponding to an instruction of the host microprocessor's instruction set, and M bits which work with the N [*1371] bits to "redefine" or "translate" the expanded RISC instruction to "emulate" the instructions of the microprocessor of the target computer. We further conclude that the claimed "expanded instruction decoder" is a decoder that "redefines" or "translates" the native instruction identified as N bits of the expanded RISC instruction, using M bits of the expanded RISC instruction, thereby enabling the instruction set of the microprocessor of the computer to emulate the instructions of a target computer.

As noted, the '927 patent defines the LHS and RHS instructions recited in claim 1, as synonymous with the N bits and M bits of the expanded RISC instruction of claims 4 and 14. The '927 patent states, "the native N bits are referred to as the LHS (left-hand side) of the instruction while the M bits are referred to as the RHS (right-hand side) of the instruction." '927 patent, col. 5, ll. 9-12. Consistent with the M+N bit expanded RISC instruction of claims 4 and 14, method claim 1 includes[**25] the step of "decoding said microcoded instruction into a LHS instruction having fields essentially compatible with a RISC architecture and a RHS instruction having fields to select a plurality of indirect registers pointing to emulated registers," and "processing said emulated registers with an arithmetic logic unit." For the reasons provided supra, we conclude that the claimed "decoding" step requires "redefining" or "translating" the native instruction, identified in claim 1 as LHS of the instruction, using the fields of the RHS of the instruction to emulate the instruction of a target computer.

II. Infringement

To support a summary judgment of noninfringement it must be shown that, on the correct claim construction, no reasonable jury could have found infringement on the undisputed facts or when all reasonable factual inferences are drawn in favor of the patentee. *Netword, LLC v. Centraal Corp., 242 F.3d 1347, 1351, 58 USPQ2d 1076, 1078 (Fed. Cir. 2001).* Similarly, "although equivalence is a factual matter normally reserved for a factfinder, the trial court should grant summary judgment in any case where no reasonable factfinder could find equivalence. [**26]" *Sage Prods. v. Devon Indus., Inc., 126 F.3d 1420, 1423, 44 USPQ2d 1103, 1106 (Fed. Cir. 1997).*

An infringement analysis is "a two-step process in which we first determine the correct claim scope, and then compare the properly construed claim to the accused device to

determine whether all of the claim limitations are present either literally or by a substantial equivalent." *Renishaw PLC v. Marposs Societa' Per Azioni, 158 F.3d 1243, 1247-48, 48 USPQ2d 1117, 1120 (Fed. Cir. 1998).* To establish literal infringement, all of the elements of the claim, as correctly construed, must be present in the accused system. See *Cole v. Kimberly-Clark Corp., 102 F.3d at 524, 532, 41 USPQ2d 1001, 1007 (Fed. Cir. 1996).*

"A party may not overcome a grant of summary judgment by merely offering conclusory statements." *Moore U.S.A., Inc. v. Standard Register Co., 229 F.3d 1091, 1112, 56 USPQ2d 1225, 1240 (Fed. Cir. 2000).* In Moore, the declarations offered by the patentee to carry its burden of proof of infringement were found insufficient. Moore's declarations alleged infringement with specific reference to the accused device. However, [**27] the Federal Circuit determined that the "allegations" contained therein were "entirely lacking in factual support." Id. This court similarly [*1372] dismissed Moore's claim of infringement under the doctrine of equivalents, finding "the mere recital of the Graver Tank mantra that the accused device performs 'the same function, in the same way, to achieve the same result,' without more, does not create a genuine issue of material fact as to whether an accused device infringes by equivalents." *Moore U.S.A., 229 F.3d at 1113, 56 USPQ2d at 1240.*

Accordingly, infringement must be shown literally or equivalently for each limitation; general assertions of facts, general denials, and conclusory statements are insufficient to shoulder the non-movant's burden. *Johnston v. IVAC Corp., 885 F.2d 1574, 1578, 12 USPQ2d 1382, 1385 (Fed. Cir. 1989)* (citing *Chemical Eng'g v. Essef Indus., 795 F.2d 1565, 230 USPQ 385 (Fed. Cir. 1986)).* Thus, the party opposing the motion for summary judgment of noninfringement must point to an evidentiary conflict created on the record, at least by a counter-statement of a fact set forth in

detail in an affidavit by a[**28] knowledgeable affiant. Mere denials or conclusory statements are insufficient. *Collins, Inc. v. N. Telecomm., Ltd., 216 F.3d 1042, 1046, 55 USPQ2d 1143, 1146 (Fed. Cir. 2000); Barmag Barmer Maschinenfabrik AG v. Murata Mach., Ltd., 731 F.2d 831, 836, 221 USPQ 561, 564 (Fed. Cir. 1984).*

In *Phillips Petroleum Co. v. Huntsman Polymers Corp., 157 F.3d 866, 48 USPQ2d 1161 (Fed. Cir. 1998),* this court held that the patentee failed, through the conclusory statements of experts, to raise a genuine issue of material fact precluding summary judgment. *157 F.3d at 876, 48 USPQ2d at 1169-70.* Rejecting Phillips' argument that the accused products contain block copolymers within the meaning of the claims, the court stated, "we agree with the Special Master's conclusion that the expert declarations are wholly conclusory, devoid of facts upon which the affiant[s'] conclusions, as experts, were reached." Id. (quotation marks omitted). Thus, unsupported or conclusory averments are insufficient to avoid summary judgment where the moving party has met its initial burden. *Celotex Corp. v. Catrett, 477 U.S. 317, 322-23, 91 L. Ed. 2d 265, 106 S. Ct. 2548 (1986);*[**29] see also *Schendel v. Curtis, 83 F.3d 1399, 1409, 38 USPQ2d 1743, 1752 (Fed. Cir. 1996).*

In accordance with the limitations of claims 4 and 14, the claimed microprocessor executes N bit "native" instructions when not emulating, and also executes M+N bit expanded instructions in an emulating mode. M bits of the instruction "redefine" the N bits corresponding to the native instruction, to create an expanded instruction that emulates the instructions of a different microprocessor. The district court concluded that "it is beyond dispute that the P6 microprocessors are not configured to emulate in the manner claimed and do not, therefore, infringe any one of the asserted claims." The court further concluded that "it is beyond question" that the P6 microprocessors do not have

both a "native mode" using microinstructions of N bits only, and an emulation mode in which the microprocessor executes M+N bit expanded instructions.

TechSearch acknowledges that the P6 microprocessor's instruction set is comprised of instructions of all "previous versions" of Intel's processors, and additional instructions newly added for the P6 microprocessor, that is, "current version" instructions. [**30] These previous version instructions [*1373]are common to both the previous version processor and the P6 processor. Because the instruction set of the P6 processor is not complete without the previous version instructions, the P6 microprocessor cannot function without those instructions.

Nor does TechSearch dispute that the P6 microprocessor executes earlier version instructions in the same manner as those from the current version or that the earlier version instructions are part of the P6 microprocessor's instruction set. On that basis, we agree that the P6 microprocessor cannot infringe. The district court correctly concluded that the P6 microprocessor does not "emulate" or modify the instructions first introduced with earlier version microprocessors when executing such previous version instructions. The P6 microprocessor cannot be said to "emulate" solely because it executes instructions that also belong to the instruction set of previous microprocessors. Those previous version instructions are part and parcel of the P6 microprocessor's instruction set.

Regardless of the version of instruction set in which an instruction was first introduced, the P6 microprocessor's instructions have[**31] the same length. Intel's processor does not operate using N bit native instructions at one time, and M+N bit expanded instructions when emulating. Nor are the M bits of the instruction ignored when the microprocessor is executing "current version" or "native" instructions.

Thus, the P6 microprocessor does not use M bits of an expanded RISC instruction, generated from an instruction which originated in a previous instruction set, to modify N bits corresponding to the current version instruction as required by the claims. Rather, the P6 microprocessor uses each bit of the previous instruction without modification, in the same manner regardless of whether the instruction originated with the P6 or an earlier version of Intel's processor. Therefore, even if we were to assume that the execution of instructions common to both the P6 and earlier version microprocessors could be deemed a form of "emulation," the instructions of the P6 microprocessor do not include M bits used to "redefine" the current version instruction to emulate an instruction of an earlier version microprocessor. Accordingly, we conclude that the district court correctly determined that no reasonable jury could find that[**32] the P6 microprocessor emulates in the manner provided in claims 4 and 14 of the *'927* patent.

The district court properly rejected Dr. Hoevel's contentions on this point. Dr. Hoevel concludes that the *'927* patent claims "[do] not require the additional presence of a 'native mode' that independently executes instructions of N bits." However, claims 4 and 14 each expressly require "a native instruction width of N bits" that is "configured for emulating." This court has stated that "the motion of an accused infringer for judgment on the ground of non-infringement of a patent may be granted where the patentee's proof is deficient in meeting an essential part of the legal standard for infringement." *Johnston v. IVAC Corp., 885 F.2d 1574, 1577, 12 USPQ2d 1382, 1384 (Fed. Cir. 1989).* We have further recognized that specific claim limitations cannot be ignored as insignificant or immaterial in determining infringement. *Perkin-Elmer Corp. v. Westinghouse Elec. Corp., 822 F.2d 1528, 1533, 3 USPQ2d 1321, 1325 (Fed. Cir. 1987).* Because Hoevel fails to recognize the native mode claim requirement, a predicate to conducting

a proper analysis of infringement, [*1374]we[**33] conclude that TechSearch has failed to raise a genuine dispute of a material fact on this issue. We conclude, therefore, that Intel was entitled to a grant of summary judgment as to noninfringment of claims 4 and 14.

Notwithstanding that the P6 microprocessor executes the earlier version instructions without modification, TechSearch argues that it produced sufficient evidence to prevent a grant of summary judgment on the issue of infringement, arguing that the "Cuops" instruction of the P6 microprocessor emulates as claimed. Based on the testimony of its expert, Dr. Hoevel, TechSearch asserts that the "Cuops" found in the P6 microprocessors used for aliasing, or register renaming, are single M+N bit expanded RISC instructions. TechSearch further argues that twenty-four bits of the Cuops instruction, including an opcode, two sources and one destination operand, are redefined using the remaining forty-nine bits that "assist in executing the instructions" of the processors.

Even assuming this "assistance" is a type of emulation, the court correctly concluded that the P6 microprocessors do not emulate "in the same way." As Dr. Hoevel recognizes, the "indirection" or register renaming[**34] performed by the P6 microprocessors "is attributable to out-of-order and superscalar complexities in the P6 that are not relevant to the '927 claims." The "emulation" identified by Dr. Hoevel is in fact aliasing for executing instructions out of order, and does not involve configuring the instruction set of a microprocessor to emulate the instruction set of another microprocessor as required by the claims. Furthermore, TechSearch does not challenge the court's conclusion that the format of the instructions that the P6 microprocessors uses when executing an instruction from an "earlier version" processor are absolutely indistinguishable from the format of the instructions exclusive to the P6 which operates in only one mode. Accordingly, we conclude that, even

assuming TechSearch has shown that some aspect of the P6 processor may be characterized as performing a form of emulation, no reasonable jury could find that the P6 emulates in the manner claimed.

As an alternative basis for finding no infringement of claims 4 and 14, the district court held that the P6 microprocessor does not have an "expanded instruction decoder" using M bits from each expanded RISC instruction to "redefine"[**35] the RISC architecture computer in terms of the target computer during emulation. Because the issue of whether the P6 includes a decoder using M bits of the expanded RISC instruction to redefine the native instruction is so intertwined with those issues relating to the M+N bit instructions addressed supra, we shall address TechSearch's arguments regarding the court's conclusions on these issues.

First, we note that TechSearch does not dispute that the "alias multiplexer," identified by TechSearch as corresponding to the claimed decoder, simply routes the inputs selectively to the outputs. The decoder of the claimed invention, on the other hand, translates the instructions into a form for processing by the ALU in a manner involving considerable processing. We find no basis to disturb the district court's conclusion that one of ordinary skill in the art would know that decoders and multiplexers perform substantially different functions and consist of substantially different structure. TechSearch has failed to dispute that fact.

Nor do we disagree with the district court's finding that Hoevel's testimony on [*1375] this issue is insufficient to raise a material issue of fact. As the court[**36] noted, Hoevel did not contend that the multiplexer in the P6 microprocessor operates as a decoder, or that the multiplexer performs the decoding as claimed. Because the claimed decoder combines input signals to produce outputs that cause selection of the direct, indirect or emulation

registers, the court correctly distinguished the operation of the alias multiplexer architecture found in the P6 on the basis that it simply steers each signal to the appropriate output field. Thus, the claimed decoding is quite different from the multiplexing found in the P6 microprocessor.

TechSearch's assertion that a multiplexer is capable of acting as a decoder does not suffice to raise a material issue of fact. Specifically, as the district court noted, TechSearch failed to provide evidence to explain how the multiplexer of the P6 performs the functions of the claimed decoder. Intel's evidence that the multiplexer does not produce outputs based on a combination of inputs stands uncontradicted. Similarly, Hoevel's wholly conclusory allegations failed to raise a genuine issue of material fact.

Nor does the multiplexer operate to "redefine" the microprocessor when "emulating." In fact, Intel's microprocessors[**37] in no way redefine instructions, much less in the manner required of the decoder recited in claims 4 and 14. The multiplexer of the P6 microprocessor does not use an additional M bits to redefine the computer when "emulating." Although Hoevel asserted that the microinstructions found in P6 microprocessors, known as "Cuops," contain fields for performing register indirection, those instructions are always the same size and always use all of their bits. Thus, no part of the Cuops microinstruction is redefined by the decoder as claimed. Therefore, the district court correctly concluded that no reasonable jury could find that the Cuops are redefined "in any way."

With regard to claim 1, the district court concluded that to prove infringement TechSearch must show 1) that the accused products, the P6 microprocessors, have "a plurality of indirect registers pointing to emulated registers," and 2) that the accused products process the emulated registers with an arithmetic logic unit. The court determined that the macro alias register file ("MAR") of the P6 microproces-

sor, alleged by TechSearch to constitute indirect registers, does not point to "any registers or to anything processed by [**38] the ALU." Rather, the MAR points to "what are known as 'logical registers,'" which are merely references and not actual registers. Thus, the court determined that the MAR does not point to registers as required by the claims.

The district court further determined that TechSearch produced no evidence that "what it considers to be the 'emulated registers' in the accused products are themselves processed" by the ALU. Thus, the court concluded that Intel was entitled to summary judgment of noninfringement of claim 1.

TechSearch argues that Intel's own documents show that logical registers are registers. Specifically, TechSearch argues that because Intel identifies logical registers as registers, the district court's conclusion that the indirect registers do not point to emulated registers is incorrect.

TechSearch asserts that at most Intel established that the logical registers of the P6 microprocessor are mapped to physical registers before processing by the ALU, in [*1376] accordance with the superscalar complexities in the P6, but TechSearch argues that this is an additional step that is not recited in the claim, and is therefore irrelevant. Similarly, TechSearch argues that the claims [**39] cannot be read to require direct processing of the data in the emulated registers by the ALU because Figure 3 of the '927 patent illustrates an embodiment where the output of the emulated registers are not processed directly by the ALU but are placed into intermediate ALU registers prior to processing.

To infringe claim 1, emulation registers in the P6 must be pointed to by indirect registers and processed by the ALU. TechSearch does not dispute that there are at least two layers of registers between the alleged indirect registers

and the alleged ALU. On that basis, we conclude that the P6 microprocessors cannot have registers both pointed to by the indirect registers and processed by the ALU, regardless of whether those registers are actually involved in emulation of a target instruction set. As TechSearch's own expert states, "Intel's indirect registers point to logical registers" and these logical registers are mapped to physical registers, which are processed by the ALU. Hoevel Declaration, P 51. As noted, Hoevel acknowledges that due to the out-of-order and superscalar complexities of the P6 processor, the P6 processor does not have emulation registers pointing to the ALU, but[**40] that an additional step of indirection is involved. Hoevel Declaration, P 51.

TechSearch counters that this additional step of indirection is irrelevant to whether the claim is infringed. We conclude, however, that where, as in this case, the claim recites steps of a method, each dependent upon the other, we cannot interpret the limitations so loosely. Rather, the claims expressly require that the indirect registers point to the emulated registers, and that the ALU processes the emulated registers.

Because TechSearch is unable to dispute that the components identified in Intel's processors as emulated registers are admittedly not both pointed to by the indirect registers and directly processed by the ALU, we cannot disturb the district court's conclusion that Intel is entitled to summary judgment on the issue of infringement. On this basis alone, we conclude that no reasonable juror could find claim 1 infringed.

The method of claim 1 requires emulation of a target computer instruction set using the RHS bits of the instruction to enable the LHS bits to emulate the instruction set of a target computer. As noted, the '927 patent defines the terms LHS and RHS, used in claim 1 and corresponding[**41] to the left-hand bits and right-hand bits of the

claimed microcoded instruction, as synonymous with the N and M bits of the expanded RISC instruction found in claims 4 and 14. '927 patent, col. 5, ll. 6-9. Claim 1 requires that a LHS of an instruction is used for executing instructions in a RISC architecture, and that the RHS is used for selecting emulated registers. Consistent with the limitations of claims 4 and 14, claim 1 further requires "[a] method for emulating the instruction set of a target computer," where that method involves the use of those "emulated registers." We conclude, therefore, in the alternative, that because no reasonable jury could find that the P6 microprocessor emulates in the manner claimed, there can be no infringement of the method recited in claim 1.

III. Appointment of a Technical Advisor

Procedural rulings are reviewed by this court under regional circuit law, [*1377]the Ninth Circuit in this case, unless the procedural issues are unique to patent law. See *Nat'l Presto v. W. Bend Co., 76 F.3d 1185, 1188 n.2, 37 USPQ2d 1685, 1686 n.2 (Fed. Cir. 1996).* Further, "we apply regional circuit law to procedural issues that are not themselves[**42] substantive patent law issues." *Bose Corp. v. JBL, Inc., 274 F.3d 1354, 1360, 61 USPQ2d 1216, 1219 (Fed. Cir. 2001); Int'l Nutrition Co. v. Horphag Research Ltd., 257 F.3d 1324, 1328, 59 USPQ2d 1532, 1535 (Fed. Cir. 2001).* The procedural issue, namely the use of a technical advisor to assist the district court in understanding complex scientific and technical factual issues, is not limited to and unique to patent cases. Technical advisors may be useful for the understanding of scientific evidence generally as well as the science or technology involved in patent cases. Because understanding issues of complex science and technology is not so unique as to clearly implicate the jurisdictional responsibilities of this court in a field within its exclusive jurisdiction, *Midwest Indus., Inc. v. Karavan Trailers, Inc., 175 F.3d 1356, 1359, 50 USPQ2d 1672, 1675*

*(Fed. Cir. 1999)* (en banc in relevant part), we apply regional procedural law. The Ninth Circuit applies the abuse of discretion standard to a district court's appointment of a technical advisor. *Ass'n of Mexican Am. Educators v. California, 231 F.3d 572, 591 (9th Cir. 2000)*[**43] (en banc).

A technical advisor is helpful in assisting the court in understanding the scientific and technical evidence it must consider. See *Id. at 590;* see also *Gen. Elec. Co. v. Joiner, 522 U.S. 136, 149, 139 L. Ed. 2d 508, 118 S. Ct. 512 (1997)* (Breyer, J., concurring) (endorsing the appointment of specialists to assist district courts in understanding scientific or technical evidence); *Reilly v. United States, 863 F.2d 149, 156 (1st Cir. 1988).* Such evidence in a patent case includes expert testimony, scientific articles and texts, and patents, upon which the court must rely in understanding the technology so that it can interpret the patent claims and determine whether to grant motions for summary judgment of validity, invalidity, infringement or noninfringement, and to assist the court in articulating appropriate jury instructions. In this case, the court specifically noted that evaluation of the prior art required it to consider and understand complex technical concepts beyond normal technical and scientific facts regularly addressed by the district court.

The district court is the gatekeeper of the trial in determining[**44] when scientific evidence is properly admissible. See *Kumho Tire Co. v. Carmichael, 526 U.S. 137, 141, 143 L. Ed. 2d 238, 119 S. Ct. 1167 (1999); Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1308 n.2, 51 USPQ2d 1161, 1168 n.2 (Fed. Cir. 1999).* Because this function is critical, the district court must have the authority to appoint a technical advisor in such instances so that the court can better understand scientific and technical evidence in order to properly discharge its gatekeeper role

of determining the admissibility of such evidence. See *Ass'n of Mexican Am. Educators, 231 F.3d at 591.* However, the federal courts of appeals must determine, the extent, if any, to which a district court has established safeguards to prevent the technical advisor from introducing new evidence and to assure that the technical advisor does not influence the district court's review of the factual disputes.

The law has long recognized that it may effectively use the knowledge of experts to inform and support the judicial process to settle disputes. The Supreme Court noted that:

[*1378] Courts have (at least in the absence of legislation[**45] to the contrary) inherent power to provide themselves with appropriate instruments required for the performance of their duties. . . . This power includes authority to appoint persons unconnected with the court to aid judges in the performance of specific judicial duties, as they may arise in the progress of a cause.

*Ex parte Peterson, 253 U.S. 300, 312, 64 L. Ed. 919, 40 S. Ct. 543 (1920).*

The trial court's inherent search for truth is the basic building block by which the judicial process maintains its credibility within the fabric of our society. In this search, it cannot be expected that trial judges will have expertise in biotechnology, microprocessor technology, organic chemistry, or other complex scientific disciplines. Therefore, in those limited cases where the scientific complexity of the technology is such that the district court may require the assistance of a technical advisor to aid in understanding the complex technology underlying the patent, it has the inherent authority to appoint such an advisor.

A district court's appointment of a technical advisor, outside of the purview of Rule 706 of the Federal Rules of Evidence, n1 falls within[**46] the district court's inherent authority, and the Ninth Circuit has held that district

courts may use technical advisors when desirable and necessary. *Ass'n of Mexican Am. Educators, 231 F.3d at 590.* It also implicitly recognized that district courts should use this inherent authority sparingly and then only in exceptionally technically complicated cases. *Id. at 590-91.* Therefore, we apply the law of the Ninth Circuit and review the appointment of the technical advisor, and whether the district court properly followed appropriate procedural safeguards, for abuse of discretion. *Id. at 591.*

n1 Courts and commentators agree that the court's inherent authority to appoint a technical advisor has not been displaced by the federal rules. See *Reilly v. United States, 863 F.2d 149, 158 (1st Cir. 1988)*; Note, Improving Judicial Gatekeeping: Technical Advisors and Scientific Evidence, *110 Harv. L. Rev. 941, 949-50 (1997).*

Although the Ninth[**47] Circuit has recognized the need for district courts to avoid impropriety, it has not held precisely what procedural safeguards district courts should employ. Thus, to establish a basis for our review, if the regional circuit court has not specifically spoken on the issue, we must reasonably predict how that court would decide the issue. *Panduit Corp. v. All States Plastic Mfg. Co., 744 F.2d 1564, 1575, 223 USPQ 465, 472 (Fed. Cir. 1984).*

In Association of Mexican American Educators, the majority noted that Judge Tashima suggested in his dissent a list of procedural safeguards. *Id. 231 F.3d at 591.* The majority did not adopt the specific guidelines delineated by the dissent because such strict compliance would unnecessarily "undo [the] entire trial" in the case before it. Id. However, it recognized the need for some procedural safeguards and the need for a reviewing court to have a standard against which to judge abuse of discretion. n2 This in the minimum implies the need to establish some definable safeguards for future [*1379] cases. Conceptually, we can

distill from the Association of Mexican American Educators opinion appropriate guidelines from which the Ninth[**48] Circuit would delineate desirable procedural mechanisms to safeguard the use of a technical advisor and generate a record for review on appeal.

n2 It is noted that through "these minimal safeguards, the parties can be assured that the technical advisor appointment process is fair and that the technical advisor does not exercise undue influence on the district court. These procedures will also enable meaningful appellate review." *Ass'n of Mexican Am. Educators, 231 F.3d at 611* (Tashima, J. dissenting); see also *id. at 614 n.9.*

These guidelines propose broad criteria for minimally safeguarding the judicial process and the district court from undue influence by the technical advisor and to ensure that the technical advisor's role is properly limited to a tutoring function and providing technical education and background information in the technology to the court. *Id. at 611-14* (Tashima, J. dissenting). In essence, the guidelines propose that the district court in[**49] appointing a technical advisor must: use a "fair and open procedure for appointing a neutral technical advisor . . . addressing any allegations of bias, partiality or lack of qualifications" in the candidates; n3 clearly define and limit the technical advisor's duties, presumably in a writing disclosed to all parties; n4 guard against extra-record information; n5 and make explicit, perhaps through a report or record, the nature and content of the technical advisor's tutelage concerning the technology. *Id. at 611.* The fact that the use of a technical advisor is permissible under such guidelines does not mean that it is invariably desirable or that safeguards are not required. As a practical matter, there is a risk that some of the judicial decision-making function will be delegated to the technical advisor. District court judges need to be extremely sensitive to this risk and minimize the potential for its occurrence. n6

n3 Typically the candidate list would be compiled through the respective parties' counsel, and through any recommendations the district court may make.

n4 One option to ensure that the technical advisor adheres to these safeguards and does not bring evidence to bear on the case would be to require pre-appointment and post-completion affidavits by the technical advisor, in which the technical advisor declares that he or she has complied with these safeguards, operated within the scope of his or her assignment, and confined his or her information sources to the record.

[**50]

n5 Typically this would entail making clear to the technical advisor that any advice he or she gives to the court cannot be based on any extra-record information, except that the advisor may rely on his or her own technology-specific knowledge and background in educating the district court.

n6 When a district court judge utilizes a technical advisor a reviewing court may want to take a hard look at the district court's decision, and to make certain that the decision does not in fact resolve factual disputes in the guise of determining that there is not a genuine issue of material fact. It has been noted that "a judge can filter out 'bad' legal advice or research from a law clerk; he or she is ill-equipped, however, to do the same with 'bad' technical advise." *Ass'n of Mexican Am. Educators, 231 F.3d at 614.* Moreover, reviewing courts may want to consider whether the procedural safeguards should be enhanced, or technical advisors should be allowed at all, when the district judge is acting as the trier of fact.

In this case, we conclude, based on the record before us, that[**51] the district court did not abuse its discretion and established sufficient protective measures to ensure that

Dr. Hearn did not unduly influence its decision. The court recognized that such appointments should be reserved for the exceptional case, but deemed it appropriate in this case because it concluded that this infringement determination was "a highly technical case far beyond the boundaries of the normal questions of fact and law with which judges routinely [*1380]grapple." The court acknowledged that technical advisors "may not contribute evidence." As such, the court properly concluded that a technical advisor is not subject to the requirements set forth in Rule 706 of the Federal Rules of Evidence regulating the appointment of expert witnesses. The district court further recognized that the technical advisor's role is limited to explaining the terminology and theory underlying the evidence offered by the parties. The court determined that its technical expert, Dr. Hearn, was a neutral third party, and explained its reasoning for that determination in its memorandum. The court assured the parties that Dr. Hearn had "agreed that he will not engage in any independent investigation of [**52] the underlying litigation, provide evidence to the Court, or contact any party or witness in this action." The court further agreed to identify any material relied upon by Dr. Hearn, other than that submitted by the parties or that "upon which a person versed in the relevant field of knowledge would be reasonably expected to rely." The court stated that Dr. Hearn would execute an affidavit indicating his understanding of that order before beginning his engagement, and would file an affidavit attesting to his compliance with its terms at the conclusion of his employment.

TechSearch complains that the district court abrogated its authority by allowing Dr. Hearn to resolve disputed issues of fact. It asserts that the district court could not have resolved the issues before it without improperly relying on the conclusions of Dr. Hearn, as evidenced by the fact that the district court had to seek the assistance of a technical advisor. TechSearch further alleges that Dr.

Hearn undertook independent research and possible experiments. It asserts that the district court likely used such information and that this created reversible error, and that the district court should have allowed the[**53] parties to depose Dr. Hearn consistent with Fed. R. Evid. 706 to determine the extent this alleged evidence influenced the court. TechSearch's allegations of independent research and experimentations stem from, inter alia, the fact that Dr. Hearn purchased computer equipment and software while a technical advisor to the court. On that basis alone, TechSearch speculates that Dr. Hearn must have been conducting independent experiments on microprocessor architecture. That Dr. Hearn billed his time to "research" and charged the court for calls he had placed, is the foundation upon which TechSearch bases its allegation of independent research. Finally, TechSearch alleges that Dr. Hearn's failure to certify his compliance with the order was reversible error.

TechSearch's arguments are without merit. As noted, the district court appointed Dr. Hearn as a technical advisor. Rule 706 applies to expert witnesses, but not to technical advisors. Unlike a technical advisor, an expert witness appointed by the court may be relied upon "as a source of evidence" and may be called upon to testify. *Ass'n of Mexican Am. Educators, 231 F.3d at 591.* Such was not the case here. Accordingly, [**54] we reject TechSearch's argument that the district court's failure to subject Dr. Hearn to cross-examination by the parties constitutes reversible error.

Upon review of the record before us, we are not convinced that the evidence suggests that Dr. Hearn conducted independent experiments or research. Nor are we persuaded that the evidence establishes that Dr. Hearn's failure to certify his compliance with the order was reversible error. As noted, the court exercised great [*1381] care to insure that Dr. Hearn's assistance did not unduly influence the

court's consideration of the evidence. To the extent the procedures followed by the district court fell somewhat short of those essential to avoiding such influence, we note that the district court appointed the technical advisor prior to the issuance of the Ninth Circuit's en banc opinion in Association of Mexican American Educators, and the district court at least followed the minimum requirements necessary at that time. Given the extent of the safeguards imposed by the district court as it exercised due care to avoid improper influence by its technical advisor, we conclude that the district court did not abuse its discretion in the appointment[**55] and use of the technical advisor.

CONCLUSION

We agree with the claim construction articulated by the district court. We further conclude that the district court properly granted Intel's motion for summary judgment of noninfringement. We also conclude that the district court did not abuse its discretion in the use of a technical advisor. Accordingly, the judgment of the district court is

AFFIRMED.

COSTS

No costs.

CONCUR BY: DYK

CONCUR:

DYK, Circuit Judge, concurring.

I join parts I and III of the majority opinion and its excellent treatment of the technical advisor issue—with one qualification. My one qualification is that I am concerned that district court judges may have a tendency to rely on technical advisors in summary judgment situations to resolve disputed issues of fact. Since we review the grant of summary judgment without deference, it can be argued

that such excessive reliance would be harmless error. But appellate review is not always perfect, and, as a practical matter, "common sense dictates that the trial judge's view will carry weight" even where our review is de novo. *Cybor Corp. v. FAS Techs., Inc., 138 F.3d 1448, 1462, 46 USPQ2d 1169, 1180 (Fed. Cir. 1998)*[**56] (en banc) (Plager, J., concurring). These risks with respect to the use of technical advisors make it all the more important that district judges confine technical advisors to the proper sphere—to provide advice without compromising the decision-making obligation of the district judge. As the majority recognizes, we must be particularly careful to take a "hard look" at the district court's conclusions. Ante at 33 n.6.

In this particular case I think that the district court's infringement analysis may have been too heavily influenced by the technical advisor, and that the district court may have resolved factual issues on summary judgment. However, the result the district court reached is correct, and as to each of the claims in dispute there is a ground for a finding of noninfringement that does not implicate my concerns about the use of the technical advisor. Accordingly, I join part II to the extent that it holds that (1) as to claim 1, Intel's P6 microprocessors lack emulated registers that are directly processed by an arithmetic logic unit ("ALU"); and (2) as to claims 4 and 14, Intel's P6 microprocessors lack an "expanded instruction decoder." This is sufficient to establish[**57] noninfringement as a matter of law. To establish noninfringement, Intel need only show that one limitation of each asserted claim is not met by Intel's P6 microprocessors. Rohm & [*1382] *Haas Co. v. Brotech Corp., 127 F.3d 1089, 1092, 44 USPQ2d 1459, 1462 (Fed. Cir. 1997); Laitram Corp. v. Rexnord, Inc., 939 F.2d 1533, 1535, 19 USPQ2d 1367, 1369 (Fed. Cir. 1991).*

## APPENDIX C

[Filed November 9, 1999]

DO NOT PUBLISH OR INCLUDE IN DATABASE

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

| | | |
|---|---|---|
| TECHSEARCH L.L.C. | ) | Case No. C-98-3484 WHO |
| | ) | |
| Plaintiff | ) | |
| vs. | ) | MEMORANDUM DECISION |
| | ) | AND ORDER |
| | ) | |
| INTEL CORPORATION, | ) | |
| | ) | |
| Defendant. | ) | |

In this patent infringement case, TechSearch, Inc. ("TechSearch"), owner of U.S. Patent No. 5,574,927[1]

---

[1] The '927 patent is highly technical. For example, the "Abstract" section of the patent begins:

> A RISC architecture computer configured for emulating the instruction set of a target computer to execute software written for the target computer, e.g. an Intel 80X86, a Motorola 680XO or a MIPS R3000. The apparatus is integrated with a core RISC computer to form a RISC computer that executes an expanded RISC instruction. The expanded RISC instruction contains the data fields which designate indirect registers that point to emulation registers that correspond to registers in the target computer. The width of the emulation registers is at least the width of those in the target computer.
>
> However, a field in the expanded RISC instruction restricts the emulated width to that required by a parti-

(continued...)

(the '927 patent") entitled "RISC Architecture Computer Configured for Emulation of the Instruction Set of a Target Computer," alleges that Intel Corporation ("Intel") sells products including devices that infringe the patent in suit. TechSearch alleges that Intel has infringed at least claims 1, 4, and 14 of the '927 patent by manufacturing and/or selling or offering to sell the following computers and/or processors: the Intel Pentium Pro processor, the Intel Pentium II processor and the Intel Pentium II processor with MMX technology. TechSearch further alleges that Intel has sold its microprocessors to companies like Dell Computer, IBM, Fujitsu, Toshiba, and Gateway 2000. Intel claims that it did not infringe the patent, that the patent is invalid, that TechSearch is not the proper owner of the patent, and that the patent is unenforceable. Intel counter-claimed, seeking a declaratory judgment that the patent is invalid and unenforceable, and that Intel did not infringe the '927 patent.

The Court finds this to be a highly technical case far beyond the boundaries of the normal questions of fact and law with which judges routinely grapple, and therefore has decided to appoint Dr. Anthony Hearn as a technical advisor. Dr Hearn is a Resident Consultant at RAND-Corporation in Santa Monica, California and an adjunct staff member at the IDA Center for Computing Sciences in Bowie, Maryland. His resume is hereto attached at Exhibit

---

[1] (...continued)
cular emulated instruction. Additionally, the expanded RISC instruction contains a field which designates the instruction mode for condition codes and selects logic to match the condition codes of the target computer. Target instructions are parsed and dispatched to sequences of one or more expanded RISC instructions to emulate each target instruction.

U.S. Patent No. 5,574,927 at 1.

A, and his declaration in support of his appointment as technical advisor is attached at Exhibit B.

The Court has the inherent authority to appoint a technical advisor without regard to the procedures set forth in Rule 706 of the Federal Rules of Evidence for appointing expert witnesses. *Reilly v. United States*, 863 F.2d 149, 154-155 and n.4 (1st Cir. 1988); *Ex Parte Peterson*, 253 U.S. 300, 312-14 (1920). "[S]uch appointments should be the exception and not the rule, and should be reserved for truly extraordinary cases where the introduction of outside skills and expertise, not possessed by the judge, will hasten the just adjudication of a dispute without dislodging the delicate balance of the juristic role." *Reilly*, 863 F.2d at 156. Recently, in *General Electric Co. v. Joiner*, Justice Breyer wrote separately to endorse this practice:

> [A]s cases presenting significant science-related issues have increased in number . . . judges have increasingly found in the Rules of Evidence and Civil Procedure ways to help them overcome the inherent difficulty of making determinations about complicated scientific or otherwise technical evidence. Among these techniques are . . . the appointment of special masters and specially trained law clerks.

522 U.S. 136; 118 S. Ct. 512, 520 (1997).

The Ninth Circuit quoted the above language in approving this Court's appointment of a technical advisor in *Association of Mexican-American Educators v. State of California*, Nos. 96-17131 & 97-15422, 1999 WL 976720 (9th Cir. Oct. 28, 1999) ("AMAE"). That case involved highly technical statistical analysis (psychometrics) which presented "problems of unusual complexity beyond the normal questions of fact and law with which judges routinely grapple." *Id.* at 20. There, the Court appointed a technical adviser to advise the Court through *ex parte* communications. The

Court did not rely on the technical advisor's opinions as a source of evidence, nor did the technical advisor testify; what the technical advisor did was to assist the Court in understanding the evidence submitted by the parties. *Id.* The Ninth Circuit held that the Court did not err in refusing cross examination of the technical advisor and in not requiring him to furnish an expert's report. *Id.*

Technical advisors are not witnesses, and may not contribute evidence. *Reilly*, 863 F.2d at 157. A judge may not appoint a technical advisor to brief him on legal issues, or to find facts outside the record of the case; the advisor's role is to acquaint the judge with the jargon and theory disclosed by the testimony and to help think through certain of the critical technical problems that invariably arise pretrial and during the trial. *Id.* at 158. Technical advisors are not subject to discovery or cross-examination. *See id.* at 159; *Renaud v. Martin Marietta Corp.*, 972 F.2d 304, 308 (10th Cir. 1992).

In this case, the Court urgently requires the assistance of a technical advisor because the parties' voluminous evidence in fields with which the Court is not familiar is extremely complicated. At the *Markman* hearing in August, the Court heard expert testimony from both parties regarding the microarchitecture and function of "RISC architecture computers." The Court subsequently examined the parties' papers and hearing exhibits, which detail the steps a microprocessor performs in order to emulate another computer, and the experts' statements as to how the patent would be understood by one skilled in the art. A technical advisor could have assisted the Court in a number of ways to clarify the conflicting, apparently one-sided opinions of each expert.

In order to resolve upcoming motions for partial summary judgment and any problems that may arise before, during, or after trial, the Court will again be faced with expert

testimony, scientific articles, and patents utilizing highly technical electrical engineering and microprocessor design. For example, in order to meaningfully determine whether a particular article "discloses and enables" the invention at issue, the Court must confront contradictory testimony from foremost experts in the field. Thus, the Court has been, and will be, asked to wrestle with concepts "beyond the normal questions of fact and law with which judges routinely grapple." *AMAE*, 1999 WL 976720 at *20.

In accepting this engagement, Dr. Hearn has affirmed to the Court that he is a neutral third party in regard to this action, that he has no ideological, financial or professional interest in the outcome of the litigation, and that he will respond *ex parte* to the Court to questions concerning technical or scientific terminology or theory in a manner consistent with his best understanding of relevant, generally accepted scientific knowledge. He has further affirmed that he has never had, does not presently have, and does not anticipate entering into any future financial, business or personal relationship with either litigant, including stock ownership, grant money, consulting contracts or employment, and will not do so while this action is pending. Nor will he use or seek to benefit from any confidential information that he may acquire in the course of this employment. Should Dr. Hearn become aware of any conflict or potential conflict, he has agreed to inform the Court immediately In such an event, the Court will inform the parties, and either seek their comments or terminate his engagement sua sponte.

Dr. Hearn has agreed that his communications with the Court and any information shown or provided to him by the Court in connection with this litigation are to be treated as confidential. Dr. Hearn has further agreed that he will not engage in any independent investigation of the underlying litigation, provide evidence to the Court, or contact any party or witness in this action. The Court will identify for

the parties materials, if any, used by Dr. Hearn in providing advice to the Court other than those submitted by the parties or those upon which a person versed in the relevant field of knowledge would be reasonably expected to rely.

The parties, including their experts and consultants, are ordered not to have any communication with Dr. Hearn except in the presence of the Court. Should any party contact Dr. Hearn (except to provide payment as set forth below), or should any person seek to communicate with him about the substantive issues involved in this litigation, he will inform the Court immediately of all facts and circumstances concerning such contact.

The parties have been advised that, consistent with the nature of his engagement, the Court anticipates having direct *ex parte* communications with Dr. Hearn.

Dr. Hearn shall keep track of his time and submit a monthly statement to the Court showing the hours expended. The parties are each directed to pay one-half of Dr. Hearn's compensation, which shall be $250 per hour for study and travel time and $300 per hour for Court time, plus such reasonable costs as he may incur in the performance of his duties.

Dr Hearn will execute an affidavit indicating his understanding of this Order prior to beginning his engagement. He will at the conclusion of his employment file an affidavit attesting to his compliance with the terms of this Order.

Therefore, good cause appearing,

IT IS HEREBY ORDERED that:

1. Dr. Anthony Hearn is appointed Technical Advisor to the Court in the above-entitled action for the purpose of assisting the Court in understanding all matters requiring technical expertise and skill above and beyond the normal matters routinely dealt with by the Court. During any

phase of the case, particularly during the testimony of experts, the Technical Advisor will be in Court and will confer *ex parte* with the Court from time to time. His role will be similar to that of a judicial clerk and, therefore, he will not be available for communication with or questioning by the parties. The Court will not call Dr. Hearn as a witness.

2. The Technical Advisor will be paid for his services at the rates of $250 per hour for study and travel time and $300 per hour for Court time, plus such reasonable costs as he may incur in the performance of his duties. Each side will pay one-half of his fees and costs when approved by the Court. Payments shall be made within 30 days after receipt by the parties of copies of Dr. Hearn's billing statements approved by the Court.

Dated: November 9, 1999.

/s/ William H. Orrick
William H. Orrick
United States District Judge

EXHIBIT A

**Anthony C. Hearn** **CONFIDENTIAL**

**ADDRESS**

451 -23rd Street, Santa Monica CA 90402
Telephone: (310) 394-3009
Fax: (310) 393-4818
Email: hearn@rand.org

**EDUCATION**

Ph.D., Theoretical Physics, 1962, Cambridge, England
First Class Honours Science Degree, Mathematics, 1959, Adelaide, Australia
Ordinary Science Degree, 1958, Adelaide, Australia

**PROFESSIONAL EXPERIENCE**

1998-: Resident Consultant, RAND, Santa Monica, California

1996-: Adjunct Staff Member, IDA Center for Computing Sciences, Bowie, Maryland

1990-1996: Resident Scholar for Information Sciences, RAND, Santa Monica, California

1980-1998: Senior Computer Scientist, RAND, Santa Monica, California

1974-1980: Chairman of Department of Computer Science, University of Utah, Salt Lake City, Utah

1973-1974: Director of Computer Division, University of Utah, Salt Lake City, Utah

1973-1980: Professor of Computer Science, University of Utah, Salt Lake City, Utah

1971-1978: Professor of Physics, University of Utah, Salt Lake City, Utah

1969-1971: Associate Professor of Physics, University or Utah, Salt Lake City, Utah

1965-1969: Associate Professor of Physics, Stanford University, Stanford, California

1964-1965: Senior Scientific Officer, Rutherford Laboratory, Didcot, England

1962-1964: Research Associate in Physics, Stanford University, Stanford, California

**RECENT CONSULTING AND COMMITTEE MEMBERSHIPS**

Review Board, IDA Center for Computing Sciences, Bowie Maryland, 1994 - Chair, 1996

National Research Council Board on Assessment of NIST Programs (member of Panel on Computing and Applied Mathematics 1987-92, Vice-Chairman 91-92)

National Research Council (member of committees and panels studying export control policy, 1988-1990)

National Science Foundation (member of Program Advisory Committee for Office of Advanced Scientific Computing 1984-1986, occasional panel member for Advanced Scientific Computation Division, Networking and Communication Research Infrastructure Division and Division of Computing and Computation Research, 1987- )

Lawrence Livermore National Laboratory (consultant to Magnetic Fusion Energy Computer Center, 1980-1990)

Specialist Editor for Computer Physics Communications, 1980-

Editorial Board, Impact of Computing in Science and Engineering, 1989-1993

## HONORS/PROFESSIONAL ORGANIZATIONS

Alfred P. Sloan Foundation Fellow, 1967-69

Listed in American Men and Women of Science, Who's Who in the West

ACM National Lecturer 1978-1980

SIAM National Lecturer 1976-1977

Association for Computing Machinery (Member, Elected 1966, Secretary SIGSAM, 1971-1973,

Vice-chairman SIGSAM, 1979-1981, Chairman SIGSAM, 1981-83)

American Physical Society (Member, Elected 1962)

Cambridge Philosophical Society (Fellow, Elected 1962)

## RESEARCH INTERESTS

Symbolic and algebraic computation, scientific computation, software portability, compilation, digital publication, networking.

## PUBLICATIONS

"Synchronization of Distributed Development Software," presented at the IMAC Workshop, ISAAC '99, Vancouver, Canada, June 1999 (coauthored with Arthur C. Norman).

"Computer Algebra and the World Wide Web," Proceedings of DISCO '96, Lecture Notes in Comp. Science 1128, Springer-Verlag, Berlin, 1996, 263-270.

"A Computer Algebra System based on Order-Sorted Algebra," Journ. Symb. Computation 19, 65-77 1995 (co-authored with E. Schruefer).

REDUCE User's Manual," Version 3.6, RAND, (July 1995).

"An Order-sorted Approach to Algebraic Computation," Proceedings of DISCO '93, Lecture Notes in Comp. Science 722, Springer-Verlag, Berlin, 1993, 134-144 (coauthored with E. Schruefer).

"Algebraic Computation: The Quiet Revolution," Artificial Intelligence and Mathematical Theory of Computation" (edited by V. Lifschitz), Academic Press, Inc., Boston (1991) 177-186.

"Equation Solving by Symbolic Computation," Computer Aided Proofs in Analysis, The IMA Volumes in Mathematics and its Applications, 28, Springer-Verlag, New York, 1991.

"Algebraic Computation Comes of Age," Computer Algebra Nederland Niewsbrief 6, Computer Algebra Nederland (1990) 14-27.

"Future Directions for Research in Symbolic Computation," SIAM Reports on Issues in the Mathematical Sciences, SIAM, Philadelphia (1990), (Workshop Chair, Edited by A. Boyle and B.F. Caviness).

"The REDUCE Algebraic 9omputation System," Computing Tools for Scientific Problem Solving, Academic Press (1990) 57-62.

"Global Trends in Computer Technology and Their Impact on Export Control", National Academy Press, Washington, D.C. (1988), (Committee member co-author).

"REDUCE User's Manual," Version 3.3, RAND. CP- 78 (July 1987). Translated into Japanese by H. Toshima and published by McGraw Hill Japan.

"Enlarging the REDUCE Domain of Computation," Proc. of SYMSAC '86, ACM, New York (1986), 100-106 (coauthored with R.J. Bradford, J.A. Padget and E. Schruefer).

"Optimal Evaluation of Algebraic Expressions," Proc. of AAECC-3, 392-403, published as Lecture Notes on Comp. Science, No. 229, Springer-Verlag, Berlin. 1986.

"REDUCE as a LISP Benchmark," SIGSAM Bulletin ACM, New York (1985) 19, 8-16 (coauthored with J.B. Marti).

"Structure: The Key to Improved Algebraic Computation," Proc. of the Second RIKEN International Symposium on Symbolic and Algebraic Computation by Computers, World Scientific, Singapore (1985), 215-230.

"History and Overview of CSNET," Proc. Symposium on Data Communications, ACM SIGCOMM, ACM, New York (1983) 138-145 (coauthored with P. J. Denning and C. W. Kern).

"REDUCE -A Case Study in Algebra System Development," Proc. EUROCAM '82, 263-272, published as Lecture Notes on Comp. Science, No. 144, Springer-Verlag, Berlin, 1982.

"Current Status of a Portable LISP Compiler," Proc. SIGPLAN '82 Symp. on Compiler Construction, ACM, New York (1982) 276-283 (coauthored with M. L. Griss and E. Benson).

"A Discipline in Crisis," Communications of the ACM, 24, 370-374, 1981 (coauthored with P. J. Denning, E. Feigenbaum, P. Gilmore, R. W. Ritchie, J. Traub).

"Analytic Integration by Computer," Information Processing Society of Japan 22, 639-650, 1981 coauthored with S. Watanabe).

"A Portable LISP Compiler," Software Practice and Experience 11, 541-605, 1981 (coauthored with M.L. Griss).

"Symbolic Computation and its Application to High-Energy Physics," Proc. 1980 CERN School of Computing, 390-406, CERN, Geneva, Switzerland, 1981.

"The Personal Algebra Machine," Information Processing 80 (Proc. IFIP Congress 80), 621-628, North-Holland,1980.

"A One-Pass Prettyprinter," SIGPLAN Notices 50-58, No. 12, ACM, New York, 14, 1979 (coauthored with Arthur C. Norman).

"Non-Modular Computation of Polynomial GCDs Using Trial Division," Proc. EUROSAM 79, 227-239, 72, published as Lecture Notes on Comp. Science, No. 72, Springer-Verlag, Berlin, 1979.

"A Program for the Orthogonalization of Polynomials in Two Variables using the REDUCE 2 Language," Comm. of JINR, No. P10 -11944, (in Russian), 1978 (coauthored with I. Bajla and G. A. Ososkov).

"Symbolic Computation, Past, Present and Future," Proc. of the Joint Meeting of the GI and DPG, Berlin, West Germany, Oct. 3-7, 1978.

"Standard LISP Report," SIGPLAN Notices, 48-68, No. 10, ACM, New York, 14, 1979 (coauthored with J. Marti, M. L. Griss, C. Griss).

"Applications of Symbolic Algebraic Computation," Comp. Phys. Comm. 17, 207-215, 1979 (coauthored with W. S. Brown).

"Algebraic Manipulation by Computer," Proc. Intern. Meeting on Programm. and Math. Meth. for Solving Phys. Probs., 96- 116, Dubna, USSR, 1978.

"The Structure of Algebraic Computations," Proc. of the Fourth Colloquium on Advanced Methods in Theoretical Physics, 1-15, St. Maximin, France, 1977.

"Symbolic Computation," Proc. CERN 1976 Computing School, 201-211, CERN, Geneva, Switzerland, 1976.

"A New REDUCE Model for Algebraic Simplification," Proc. SYMSAC 76, 46-52, ACM, New York, 1976.

"Scientific Applications of Symbolic Computation," Computer Science and Scientific Computation, 83-108, Academic Press, Inc., New York, 1976.

"A Mode Analyzing Algebraic Simplification Program," Proc. ACM 74, 722-724, ACM, New York, 1974.

"Polynomial and Rational Function Representations," Proc. Mathematical Software II, 211 (abstract only), Purdue University, May 29-31, 1974.

"Analytic Computation of Some Integrals in Fourth Order Quantum Electrodynamics," Journ. Compo Phys. 14 to 301-317, 1974 (coauthored with J. A. Fox).

"The REDUCE Program for Computer Algebra," Proc. Third Colloq. on Advanced Computing Methods in Theoretical Physics, CNRS, Marseilles, June, 1973.

"REDUCE 2 User's Manual," 2nd edition, 1973.

"Extended Polynomial Algorithms," Proc. ACM 73, 147-152, ACM, New York, 1973 (coauthored with R. Loos).

"A REDUCE Solution of Problem 2 -The Y(2n) Functions," SIGSAM Bulletin, pg. 14, ACM, New York, 1972.

"Comments on Problem 2 -The Y(2n) Functions," SIGSAM Bulletin, No. 15, ACM, New York, 24, 1972 (with D. Barton).

"An Improved Non-modular Polynomial GCD Algorithm," SIGSAM Bulletin, 10-15, ACM, New York 1972.

"Computer Solution of Symbolic Problems in Theoretical Physics," Computing as a Language as Physics, 567-596, IAEA, Vienna, 1972.

"The Computer Solution of Algebraic Problems by Pattern Matching," Proc. of the Second Colloquium on Advanced Computing Methods in Theoretical Physics, CNRS, Marseilles, June 21-25, 1971.

"Calculation of Traces of Products of Gamma Matrices'," Proc. of the Second Colloquium on Advanced Computing Methods in Theoretical Physics, CNRS, Marseilles, June 21-25, 1971.

"Applications of Symbolic Manipulation in Theoretical Physics," Proc. of Second Symposium on Symbolic and Algebraic Manipulation, International Hotel, Los Angeles, March 23-25, 1971, page 511, Comm. ACM 14, 1971.

"REDUCE 2, A System and Language for Algebraic Manipulation," Proc. of Second Symposium on Symbolic and Algebraic Manipulation, International Hotel, Los Angeles, March 23-25, 1971.

"REDUCE: A Program for Symbolic Algebraic Computation," Proc. of SHARE XXXIV, Denver, Colorado, March 2-6, 1970.

"REDUCE 2 User's Manual," Stratford Artificial Intelligence Project Memo, AIM-133, October 1970.

"Computer Solution of Algebraic Problems in Theoretical Physics," Proc. of the Joint Conference on Mathematical and Computer Aids to Design, Disneyland, Anaheim, California, October 27-31, 1970.

"Symbolic Analysis of Feymnan Diagrams by Computer," J. Computational Physics 5, 280, 1970 (coauthored with J. A. Campbell).

"Determination of the Real Part of the Compton Amplitude at a Nuclear Resonance," Phys. Rev. 187,1899, 1969, (co-authored with S. J. Brodsky and R. G. Parsons).

"STANDARD LISP," SIGPLAN Notices, ACM, New York, 4, No.9 (Sept. 69). Reprinted in SIGSAM Bulletin 28-49, ACM, New York, 13, 1969.

adiative Corrections to an Electron-Position Scattering Experiment," Phys. Rev. 187, 1950, 1969, (coauthored with P. K. Kuo and D. R. Yennie).

"The Problem of Substitution," Proc. of the IBM Summer Institute on Symbolic Mathematics by Computer, July-August 1968, IBM Programming Laboratory Report No. FSC-69-0312 (edited by R. G. obey, June 1969).

"REDUCE - A User Oriented Interactive System for Algebraic Simplification," Interactive Systems for Experimental Applied Mathematics, pp. 79-90 (edited by M. Klerer and J. Reinfelds, Academic Press, New York, 1968).

"REDUCE User's Manual," Institute of Theoretical Physics, Department of Physics, Stanford University, Report No. ITP- 292, 1967, rev. 1968.

"Peripheral Processes," High Energy Physics, Vol. II, p. 219 (edited by E. H. S. Burhop, Academic Press, New York, 1967), (coauthored with S. D. Drell).

"Computation of Algebraic Properties of Elementary Particle Reactions Using a Digital Computer," Communications of the ACM, No.9, p. 573-577, 1966.

"Exact Sum Rule for Nucleon Magnetic Moments," Phys. Rev. Letters, 16, 908, 1966. Reprinted in S. L. Adler and R. F. Dashen, "Current Algebras and Applications to Particle Physics," W. A. Benjamin, 1968 (coauthored with S. D. Drell).

"Differential Cross Section for e+ + e- -> W+ + W- -> e- + nubar(e) + mu+ + nu(mu)," Phys. Rev. 140, B721, 1966 (coauthored with Y. S. Tsai). A summary of this paper may be found in the Proc. of the International Symposium on Election and Photon Interactions at High Energies, Hamburg, II, 320, 1965.

"Backward Anomaly in pi0 Photoproduction," Proc. of the International Symposium on Electron and Photon Interactions at High Energies, p. 292, Hamburg, II, 1965 (coauthored with C. Schaerf).

"Photoproduction of piO from Hydrogen near the Second Pion-Nuclear Resonance," Phys. Rev. 140, B336: 1965 (coauthored with H. DeStaebler, Jr., E. F. Erickson and C. Schaerf).

"Bounds on Propagators, Coupling Constants and Vertex Functions," Phys. Rev. 136, B1439, 1964 (coauthored with S. D. Drell and A. C. Finn).

"Theory of Proton Compton Scattering," Proc. of the International Conference on Nucleon Structure, Stanford University, pp. 314-315, Stanford University Press, 1963 (coauthored with E. Leader).

"Fixed Angle Dispersion Relations for Nucleon Compton Scattering, 1," Physics Rev. 126, p. 789, 1962 (coauthored with E. Leader).

"The Invariant Amplitudes of Interaction Processes," Nuovo Cimento 21, p. 333, 1961.

*June* 1999

Exhibit B

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

| | | |
|---|---|---|
| TECHSEARCH L.L.C., | ) | Case No. C-98-3484 WHO |
| | ) | |
| Plaintiff, | ) | DECLARATION OF DR. |
| v. | ) | ANTHONY C. HEARN |
| | ) | IN SUPPORT OF |
| | ) | APPOINTMENT AS |
| INTEL CORPORATION, | ) | COURT TECHNICAL |
| | ) | ADVISOR |
| Defendant. | ) | |

I, Dr. Anthony Hearn, declare under penalty of perjury under the laws of the United States as follows:

1. I agree to act as the Court's technical Advisor in this action. I will assist the Court in educating itself in the terminology and theory disclosed by the evidence as the Court deems necessary. I will act as a sounding board for the Court to think through the scientific significance of the evidence, and will assist the Court in understanding any technological evidence, hypothesis or theory on which the experts base their testimony. In so doing, I will to the best of my ability respond in a manner consistent with generally accepted knowledge in the relevant area.

2. I understand and agree that I am not to engage in any independent investigation of the litigation, provide evidence to the Court, or contact any party or witness in this action.

3. I hereby certify that I have read and that I understand the terms of the Protective Order between TechSearch, Inc., and Intel Corporation, and agree to be bound by its terms. I understand and agree that my communications with the Court on this matter and any information shown or pro-

vided to me by the Court are to be treated as confidential. I understand that this requirement of confidentiality shall not apply to the fact of my engagement, the amount of compensation I receive, information available to me from public records, or any matter otherwise specified in writing by the Court.

4. I affirm that the declaration and Curriculum Vitae provided by me to the Court was accurate and complete in all material respects.

5. I affirm that I am a neutral third party in regard to this action, with no ideological, financial or professional interest in the outcome of the litigation.

6. I affirm that I have never had nor presently have, nor anticipate in the future having any financial, business or personal relationship with either party, including stock ownership, grant money, consulting or employment.

7. I agree that I will not acquire any stock in either party until final resolution of this action, nor use or seek to benefit from any confidential information I may acquire in the course of this engagement.

8. I understand and agree that if I become aware of any conflict or potential conflict, I am to inform the Court immediately.

9. I understand and agree that should any party contact me (except to provide payment as set forth in the Order), or should any person seek to communicate with me about any substantive issue in this litigation, I will inform the Court immediately of all facts and circumstances concerning such contact.

10. I agree to keep accurate records of my time and submit a monthly statement for the Court's approval showing the hours I have expended on matters referred to me by the Court.

I declare under penalty of perjury under the laws of the United States that the foregoing is true and correct.

Executed on November 9, 1999.

/s/ Anthony C. Hearn
Dr. Anthony C. Hearn

## APPENDIX D

[Filed February 3, 2000]

**DO NOT PUBLISH OR INCLUDE IN DATABASE**

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

| | | |
|---|---|---|
| TECHSEARCH L.L.C., | ) | |
| | ) | |
| Plaintiff, | ) | No. C-98-3484 WHO |
| vs. | ) | |
| | ) | ORDER |
| | ) | |
| INTEL CORPORATION, | ) | |
| | ) | |
| Defendant. | ) | |
| | ) | |
| | ) | |
| AND RELATED COUNTERCLAIM. | ) | |
| | ) | |

Dr. Anthony C. Hearn having submitted to the Court his statements for services rendered and expenses ("Exhibit A") in the amount of $19,157.97,

IT IS HEREBY ORDERED that pursuant to the Court's Order filed November 12, 1999, TechSearch L.L.C. and Intel Corporation shall each pay *forthwith* the sum of $9,578.98 to Dr. Anthony C. Hearn as payment as of his fees and expenses from October 24, 1999 through December 23, 1999.

Dated: February 3, 2000.

/s/ William H. Orrick
William H. Orrick
United States District Judge

App. 68

Exhibit A

**Anthony C. Hearn**
**SSN 572-66-0427**
**451 - 23rd Street**
**Santa Monica CA 90402**

December 2, 1999

INVOICE

Expenses in connection with service
as Court Technical Advisor for
U.S. District Court Case No. C 98 03484 WHO,
*TechSearch L.L.C. v. Intel Corporation*

October 24, 1999 - November 30, 1999

| Date | Item | Amount |
|---|---|---|
| 10/24/99 | Research, 2 hours | $500.00 |
| 11/02/99 | Research, 2 hours | 500.00 |
| 11/03/99 | Private auto from home to LAX, 12 miles @ 31c/mile | 3.72 |
| 11/03/99 | Air fare, LAX - SFO - LAX (receipt enclosed) | 222.54 |
| 11/03/99 | Phone call to Judge from plane (receipt enclosed) | 10.41 |
| 11/03/99 | Transportation to downtown San Francisco | 20.00 |
| 11/03/99 | Travel time, Santa Monica to San Francisco, 4 hours | 1000.00 |
| 11/03/99 | Research discussions with Judge and staff, 4.5 hours | 1125.00 |
| 11/03/99 | Transportation to SFO (receipt enclosed) | 31.00 |

| | | |
|---|---|---|
| 11/03/99 | Travel time, San Francisco to Santa Monica, 3.5 hours | 875.00 |
| 11/03/99 | LAX parking (receipt enclosed) | 13.00 |
| 11/03/99 | Private auto from LAX to home, 12 miles @ 31c/mile | 3.72 |
| 11/09/99 | Postage | 3.20 |
| 11/17/99 | Research, 1.5 hours | 375.00 |
| 11/18/99 | Research, 2 hours | 500.00 |
| 11/19/99 | Research, 2 hours | 500.00 |
| 11/20/99 | Research, 2 hours | 500.00 |
| 11/21/99 | Research, 2 hours | 500.00 |
| 11/22/99 | Research, 2 hours | 500.00 |
| 11/23/99 | Research, 2 hours | 500.00 |
| 11/29/99 | Research, 3 hours | 750.00 |
| 11/30/99 | Research, 2 hours | 500.00 |
| | **Total** | **$8932.59** |

**Anthony C. Hearn**
**SSN 572-66-0427**
**451 - 23rd Street**
**Santa Monica CA 90402**

January 3, 2000

INVOICE

Expenses in connection with service as
Court Technical Advisor for
U.S. District Court Case No. C 98 03484 WHO,
*TechSearch L.L.C. v. Intel Corporation*

December 1, 1999 - December 31, 1999

**Professional Services**

| Date | Item | Amount |
|---|---|---|
| 12/1/99 | Research, 3 hours | $750.00 |
| 12/2/99 | Research, 3 hours | 750.00 |
| 12/3/99 | Research, 3 hours | 750.00 |
| 12/4/99 | Research, 3 hours | 750.00 |
| 12/12/99 | Research, 1.5 hours | 375.00 |
| 12/13/99 | Travel time, Santa Monica to San Francisco, 3.5 hours | 875.00 |
| 12/13/99 | Research discussions, 3 hours | 750.00 |
| 12/14/99 | Research discussions, 4 hours | 1000.00 |
| 12/14/99 | Court attendance, 3.5 hours | 1050.00 |
| 12/14/99 | Travel time, San Francisco to Santa Monica, 3 hours | 750.00 |
| 12/15/99 | Research, 2 hours | 500.00 |
| 12/20/99 | Research, 2 hours | 500.00 |
| 12/21/99 | Research, 2 hours | 500.00 |
| 12/23/99 | Research, 2 hours | 500.00 |
| | **Total** | **9800.00** |

**Expenses**

| Date | Item | Amount |
|---|---|---|
| 12/13/99 | Private auto from home to LAX, 12 miles @ 31c/mile | 3.72 |
| 12/13/99 | Air fare, LAX-SFO-LAX (receipt enclosed) | 222.54 |
| 12/13/99 | Taxi to downtown San Francisco (receipt enclosed) | 31.00 |
| 12/13/99 | Lunch | 11.50 |
| 12/13/99 | Dinner (receipt enclosed) | 37.50 |
| 12/14/99 | Hotel (receipt enclosed) | 85.50 |
| 12/14/99 | Taxi to SFO (receipt enclosed) | 32.00 |
| 12/14/99 | LAX parking (receipt enclosed) | 15.40 |
| 12/14/99 | Private auto from LAX to home, 12 miles @ 31c/mile | 3.72 |
| various | Phone calls | 12.50 |
| | **Total** | **455.38** |
| | **GRAND TOTAL** | **$10225.38** |

UNITED MILEAGE PLUS
VISA/MASTERCARD

FIRST USA

Closing Date 11/8/99

## Transactions

| Trans. Date | Post Date | Description | Reference Number | Debits | Credit |
|---|---|---|---|---|---|
| 10/28 | 10/28 | Barnes & Noble.com | 24610439F2ENBG3L8 | 58.70 | |
| 10/29 | 10/29 | Avis Rental Car | 24138299FMQM7RPDX | 231.36 | |
| 10/29 | 10/29 | Crown 11914120 | 24299109F3A45V28H | 10.95 | |
| 10/29 | 10/29 | Residence Inn | 24610439F0Y1K88G3 | 621.60 | |
| 10/29 | 10/29 | United Air | 24792629JHNGWVG40 | 125.00 | |
| 10/31 | 10/31 | Best Buy | 24399009G8KL037HN | 86.58 | |
| 11/02 | 11/02 | UNOCAL 76 | 24164079J6D6505BA | 17.80 | |
| 11/03 | 11/03 | LA Airport Parking | 24092759MS662ZQBE | 13.00 | |
| 11/03 | 11/03 | GTE Air | 2460439M07VZASJK | 10.41 | |
| 11/03 | 11/05 | Regal Carpet | 24789169MFBQ9TAKO | 793.00 | |
| 11/04 | 11/05 | Economy Glass Co | 24656549PWGYJ26RY | 84.95 | |
| 11/05 | 11/05 | Best Internet Com. | 24492809M3QA7YH1J | 24.00 | |
| 11/05 | 11/05 | Creative Computers | 24692169N00L9M8R4 | 5.95 | |
| 11/05 | 11/05 | United Air | 24792629NKV2H1QVS | 331.38 | |
| 11/06 | 11/06 | Patty's Presto | 24246519P3MB3L08V | 11.95 | |
| 11/06 | 11/06 | Fry's Electronics | 24492159PNQ695WZW | 218.59 | |
| 11/06 | 11/06 | Creative Computers | 24692169P00LNGTMN | 18.39 | |

## APPENDIX E

[Filed February 16, 2000]

**DO NOT PUBLISH OR INCLUDE IN DATABASE**

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

| | | |
|---|---|---|
| TECHSEARCH L.L.C., | ) | |
| | ) | |
| Plaintiff, | ) | No. C-98-3484 WHO |
| vs. | ) | |
| | ) | ORDER |
| | ) | |
| INTEL CORPORATION, | ) | |
| | ) | |
| Defendant. | ) | |
| | ) | |
| | ) | |
| AND RELATED COUNTERCLAIM. | ) | |
| | ) | |

Dr. Anthony C. Hearn having submitted to the Court his statement for services rendered ("Exhibit A") in the amount of $1,500,

IT IS HEREBY ORDERED that pursuant to the Court's Order filed November 12, 1999, TechSearch L.L.C. and Intel Corporation shall each pay *forthwith* the sum of $750.00 to Dr. Anthony C. Hearn as payment of his fees from January 3 through January 23, 2000.

Dated: February 16, 2000.

/s/ William H. Orrick
William H. Orrick
United States District Judge

App. 74

Exhibit A

**Anthony C. Hearn**
**SSN 572-66-0427**
**451 - 23rd Street**
**Santa Monica CA 90402**

February 2, 2000

INVOICE

Expenses in connection with service as
Court Technical Advisor for
U.S. District Court Case No. C 98 03484 WHO,
*TechSearch L.L.C. v. Intel Corporation*

January 1, 2000 - January 31, 2000

**Professional Services**

| Date | Item | Amount |
|---|---|---|
| 1/3/00 | Research, 0.5 hour | $125.00 |
| 1/11/00 | Research, 1 hour | 250.00 |
| 1/12/00 | Research, 1 hour | 250.00 |
| 1/13/00 | Research, 0.5 hour | 125.00 |
| 1/20/00 | Research, 0.5 hour | 125.00 |
| 1/21/00 | Research, 1.5 hours | 375.00 |
| 1/23/00 | Research, 1 hour | 250.00 |
| | **TOTAL** | **$1500.00** |

**APPENDIX F**

[Filed January 31, 2000]

**DO NOT PUBLISH OR INCLUDE IN DATABASE**

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

| | |
|---|---|
| TECHSEARCH L.L.C.<br><br>Plaintiff<br><br>vs.<br><br>INTEL CORPORATION,<br><br>Defendant.<br><br>AND RELATED COUNTERCLAIM. | No. C 98-03484 WHO<br><br>MEMORANDUM<br>DECISION<br>AND ORDER |

In this patent infringement action brought by plaintiff TechSearch L.L.C. ("TechSearch") against defendant Intel Corporation ("Intel"), Intel filed various motions for summary judgment against TechSearch, claiming that the patent-in-suit is anticipated by prior art, that four of Intel's patents are prior art, that the patent-in-suit is not infringed, and that the patent is invalid. TechSearch filed cross-motions for summary judgment, claiming that the patent is enforceable and not anticipated.

After considering the submissions on file and arguments of counsel, the Court finds that Intel's accused products do not infringe the patent-in-suit. Because the determination of noninfringement is dispositive, the Court does not reach

the merits of the parties' other motions for summary judgment,[1] and dismisses them as moot.[2]

I.

The parties' joint statement of undisputed facts ("UF") does not include any facts pertaining to the background of this litigation. This statement of facts is, therefore, necessarily gleaned from the voluminous submissions of the parties.[3] On March 25, 1994, the application for U.S. Patent No. 5,574,927 (the '927 patent) was filed. (UF at 1:7-8.) The

---

[1] The parties have filed a total of eight motions for summary judgment on issues regarding the validity and enforceability of the patent-in-suit and whether Intel's accused products infringe the patent-in-suit. The motions are as follows: (1) Intel's motion for summary judgment of invalidity, (2) Intel's motion for partial summary judgment regarding prior art under 35 U.S.C. § 102(e), (3) Intel's motion for summary judgment of invalidity based on anticipation by the registration of the 3250 product description with the copyright office, (4) Intel's motion for summary judgment of invalidity based on on-sale bar violation and best mode violation, (5) Intel's motion for summary judgment of noninfringement, (6) TechSearch's motion for summary judgment of enforceability, (7) Intel's countermotion for summary judgment of unenforceability, and (8) TechSearch's motion for summary judgment that none of Intel's asserted prior art anticipates the patent-in-suit.

[2] Intel's counterclaim for declaratory relief is also dismissed as moot. *Phonometrics, Inc. v. Northern Telecom Inc.*, 133 F.3d 1459 (Fed. Cir. 1998) (holding that district court's decision to dismiss as moot the counterclaim of patent invalidity was within the court's discretion after granting summary judgment of noninfringement).

[3] This statement of facts does not include irrelevant factual matters that do not bear on the disposition of the infringement question, including the events surrounding a Texas bankruptcy proceeding involving IMS.

patent was issued on November 12, 1996. (Greenspoon Decl. Ex. 1, U.S. Patent No. 5,574,927.[4]) The names inventor is Henry L. Scantlin ("Scantlin"); Scantlin subsequently assigned the '927 patent to International Meta Systems, Inc. ("IMS"), his employer. The patent is entitled "RISC Architecture Computer Configured for Emulation of the Instruction Set of a Target Computer."[5] In the early 1990's, IMS sought to develop and manufacture a microprocessor known as the "IMS 3250," a microchip design that evolved over time; a version of this microprocessor, the "3250B," is identified as the preferred embodiment of the invention claimed in the '927 patent. Ultimately, after working on several versions of the 3250, IMS's attempts to produce the microprocessor commercially failed, and IMS sold the '927 patent to TechSearch for $50,000 plus ten percent of the proceeds of subsequent litigation involving the patent.

Stated simply, the invention claimed in the '927 patent describes a computer that is cheaper to build and more flexible than several popular computers. The patent covers certain microprocessors that are able to copy, or "emulate," the internal instructions of other microprocessors (specifically, Intel's Pentium chips, among others) so that they can perform the functions of those microprocessors more efficiently.

TechSearch contends that Intel's P6 line of microprocessors ("the accused products") infringe the microprocessors in its '927 patent. TechSearch filed a complaint alleging patent infringement in the Northern District of Illinois. On September 14, 1998, the case was transferred to the

---

[4] Hereafter cited as the "'927 patent."

[5] The acronym RISC stands for "Reduced Instruction Set Computer." For a more detailed explanation of RISC versus CISC ("Complex Instruction Set Computer"), see the Memorandum Decision and Order filed November 1, 1999, at pages 5-6.

Northern District of California. On March 5, 1999, Intel moved for summary judgment of invalidity. The Court postponed ruling on Intel's summary judgment motion until after it construed claims 1,4, and 14 of the '927 patent. The Court held a *Markman* hearing on August 10, 1999, and issued its Memorandum Decision and order (hereafter "Claim Construction Order") on November 1, 1999. The parties then filed the present cross-motions for summary judgment.

In its motion for summary judgment of noninfringement, Intel establishes beyond doubt and without cavil that its P6 microprocessor line is substantially different in material respects from the subject matter claimed in claims 1, 4, and 14 of the '927 patent. The Court, therefore, finds that Intel's products do not infringe claims 1, 4, or 14 literally or under the doctrine of equivalents, as discussed below.[6]

---

[6] Intel also filed an *ex parte* motion to strike eight declarations submitted by TechSearch in opposition to Intel's various motions for summary judgment. Only one of those declarations is relevant to the motion for summary judgment of noninfringement: the declaration of Dr. Lee Hoevel in opposition to Intel's motion for summary judgment of noninfringement dated November 22, 1999. The Court declines to rule on whether to strike the other declarations because they relate to motions not reached by the Court. Intel contends that Dr. Hoevel's declaration opposing Intel's motion for summary judgment contains new opinions and bases for opinions regarding infringement that go beyond Dr. Hoevel's expert report pursuant to Rule 26(a) (2) of the Federal Rules of Civil Procedure. After comparing Dr. Hoevel's expert report and supplement (Reines Decl. in Support of Intel's Ex Parte Motion to Strike, Exs. N & 0) with his declaration in opposition to summary judgment (*Id.* Ex. M), the Court finds that Dr. Hoevel's expert report and supplement sufficiently set forth the theories of infringement expanded upon in the November 22, 1999 declaration. Intel's *ex parte* motion to strike is, therefore, denied as to Dr.

(continued...)

II.

A.

In determining patent infringement, the Court applies a two-step analysis: (1) determining the proper construction of the claims, which is a matter of law, and (2) determining whether a particular device infringes a properly construed claim, which is a question of fact. *Wright Med. Tech., Inc. v. Osteonics Corp.*, 122 F.3d 1440, 1443 (Fed. Cir. 1997). Literal infringement occurs if each of the limitations in the asserted claim is found in the accused device. *Id.* "Demonstration that every limitation of the claim is literally met by the accused device must be shown by a preponderance of the evidence." *Kahn v. General Motors Corg.*, 135 F.3d 1472, 1476 (Fed. Cir. 1998) (citation omitted).

Infringement also may be found under the doctrine of equivalents. Under the doctrine of equivalents, an accused device that does not literally infringe upon the express terms of a patent claim may nonetheless be found to infringe if there is equivalence between the elements of the accused product or process and the claimed elements of the patented invention. *Id.* at 1478 (quoting *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 40 (1997). The doctrine of equivalents applies "when, absent estoppel, every limitation of the asserted claim, or its equivalent, is found in the accused subject matter, the latter differs from what is literally claimed only insubstantially, and it performs substantially the same function in substantially the same way to achieve substantially the same result." *Wright Med. Tech.*, 122 F.3d at 1444 (citing *Warner-Jenkinson Co.*,

---

[6] (...continued)
Hoevel's declaration in opposition to Intel's motion for summary judgment of noninfringement. Because the determination that the accused products do not infringe the patent is dispositive, the Court declines to rule on the balance of the motion to strike.

520 U.S. at 40-41); *Graver Tank & Mfg. Co. v. Linde Air Prods. Co.*, 339 U.S. 605, 608-09 (1950). Here, because the Court has already construed the claims, the only remaining issue is whether every limitation in the claims is or is not present in the accused device, either literally or by the doctrine of equivalents.

Summary judgment on the issue of literal noninfringement is appropriate when "no reasonable jury could find that every limitation recited in the properly construed claim either is or is not found in the accused device." *Bai v. L & L Wings, Inc.*, 160 F.3d 1350, 1353 (Fed. Cir. 1998) (citations omitted). As a matter of law, an accused device cannot infringe if even a single limitation is not satisfied. *Digital Biometrics, Inc. v. Identix, Inc.*, 149 F.3d 1335, 1349 (Fed. Cir. 1998). In addition, the Supreme Court has directed courts to employ "special vigilance" to prevent the doctrine of equivalents from eliminating claim elements. *Warner-Jenkinson Co.*, 520 U.S. 17. The Federal Circuit has observed this guidance in affirming the grant of summary judgment to dispose of infringement claims under the doctrine of equivalents when no reasonable jury could determine two elements to be equivalent. *Phillips Petroleum Co. v. Huntsman Polymers Corp.*, 157 F.3d 866 (Fed. Cir. 1998); *Loral Fairchild Corp. v. Sony Corp.*, 181 F.3d 1313 (Fed. Cir. 1999). The inclusion of one or more additional structures to steps, however, cannot avoid infringement where all of the structure steps required by the claims are present. *Amster Corp. v. Envirotech Corp.*, 730 F.2d 1476, 1482 (Fed. Cir. 1984). Even later technological advances or embellishments that were unknown at the time a patent issued may be covered by the claims of the patent-in-suit. *Kinzenbaw v. Deere & Co.*, 741 F.2d 383, 389 (Fed. Cir. 1984).

The intent of the allegedly infringing party has no relevance to the inquiry. *Warner-Jenkinson Co.*, 520 U.S. at 35.

Rather, the essential inquiry is: "Does the accused product or process contain elements identical or equivalent to each claimed element of the patented invention?" *Id.* at 19.

B.

Before turning to the merits of Intel's motion for summary judgment of noninfringement, the Court preliminarily notes that one of Intel's central claims is that the accused products do not infringe claims 1, 4, and 14 because they are not RISC architecture computers. Specifically, Intel asserts that P6 microprocessors are not RISC because (1) the microinstructions are not RISC, (2) they do not have a "relatively small set of microinstructions," (3) they do not have simple microinstructions, and (4) their microinstructions are not processed "generally within a single clock cycle."[7] The Court will not address the merits of this particular claim; as noted in the Claim Construction Order, the RISC/CISC distinction is an unusually complicated one in the context of this particular patent and need not be determined in order to decide whether the patent-in-suit has been infringed. (Claim Construction Order at 12-13 & n.8.) Because there are other reasons showing conclusively that the accused devices do not infringe the '927 patent, the Court will instead address Intel's other noninfringement arguments.

---

[7] A "clock cycle" refers to the speed at which the internal clock in an electronic device oscillates. "In computers, each tick (oscillation) of the clock is called a cycle, and the clock rate is measured in megahertz, or millions of cycles per second." Microsoft Computer Dictionary at 89 (4th ed. 1999) (included in definition of "clock rate").

1.

Intel first argues that the accused products do not infringe claim 1 of the patent because they do not perform steps 4 and 5, namely, "decoding said microcoded instructions into a LHS[8] instruction having fields essentially compatible with a RISC architecture and a RHS instruction having fields to select a plurality of indirect registers pointing to emulated registers,"[9] and "processing said emulated registers with an arithmetic logic unit."[10] ('927 patent at 53:7-13.) To prove infringement of claim 1, TechSearch must show that the P6's have "a plurality of indirect registers pointing to emulated registers," and that the accused products process the emulated registers with an arithmetic logic unit. TechSearch claims that the macro alias register file ("MAR") in the P6 microprocessors constitutes a plurality of indirect registers. (Techsearch's Opp'n at 21). Even assuming this to be true, however, the P6 cannot satisfy this claim element because the MAR does not point to emulated registers as required. Further, there

---

[8] The '927 patent divides each computer instruction into two parts, referred to as a "LHS" (left-hand side) and a "RHS" (right-hand side). The LHS contains references to the underlying RISC instructions of the host computer and the RHS to the instructions of the target computer.

[9] A register is "[a] set of bits of high-speed memory within a microprocessor . . . used to hold data for a particular purpose." Microsoft Computer Dictionary at 379 (4th ed. 1999). An indirect register is a particular form of register that points to another register rather than direct data. In the '927 patent, the indirect registers select the relevant emulation registers. ('927 patent at 53:41.)

[10] An arithmetic logic unit is a component of a computer's central processing unit that performs arithmetic operations such as addition, subtraction and multiplication, as well as basic logical operations.

are no registers in the P6 microprocessors that are both pointed to by the indirect registers and processed with an arithmetic logic unit. (Papworth Decl. at ¶29; Reines Corrected Decl. Ex. A, Flynn Rebuttal Rep. at 24-25.) Put simply, the MAR does not point to any registers (*id.*), nor does it point to anything that is ever processed by the arithmetic logic unit in the P6 microprocessors. The MAR points to what are known as "logical registers," which are not actual registers, but merely references. (*Id.*) Finally, TechSearch has produced no evidence that what it considers to be the "emulated registers" in the accused products are themselves processed. Intel is, therefore, entitled to summary judgment of noninfringement of claim 1 of the '927 patent, under both the doctrine of literal infringement and the doctrine of equivalents.

2.

Intel next argues that the accused products do not infringe because they are not "configured to emulate the instruction set of a target computer" as required by the patent.[11] The '927 patent discloses and claims a RISC architecture computer that is configured to emulate the instruction set of a target computer. The Court finds that it is beyond dispute that the P6 microprocessors are not configured to emulate in the manner claimed and do not, therefore, infringe anyone of the asserted claims. Indeed, as a general matter, the invention in the '927 patent is di-

---

[11] Claim 1 claims a method for "emulating the instruction set of a target computer" comprising 9 steps, and the preambles of claims 4 and 14 recite "[a] RISC architecture computer having a native instruction width of N bits configured for emulating target instructions from the instruction set of a target computer, comprising . . . ." ('927 patent at 52:65-67, 53:33-36, 54:2-24.)

rected toward making emulation easy, while the P6 design is not so specifically directed.

Each of the asserted claims contemplates that a computer have certain characteristics in emulation mode, and that the computer is capable of functioning when it is not emulating. Specifically, the "N bits" (in claims 4 and 14) "define[ ] the number of bits in the native instruction of the microprocessor when it is not in emulation mode." (Claim Construction Order at 16-17; *id.* at 30-31 ("N bits defines the instruction when the microprocessor is not in emulation mode.").)

The "patent specification makes clear that its emulation scheme entails modifying preexisting native instructions of a RISC architecture computer." (*Id.* at 21:3-5 (citing '927 patent at 5:3-12).) When the computer is emulating, the native instructions are redefined by M bits in order to form an M+N bit expanded instruction that enables the host system to emulate the target system. (*Id.* at 18:9-12.) In other words, when not emulating, the computer's microinstructions will have a native instruction width of N bits, and when emulating, the computer's microinstructions will be expanded to M+N. The Court held that both the "native instruction width of N bits" and the M+N expanded instruction are claim limitations. (*Id.* at 21, 31.)

In order to demonstrate infringement of claims 4 and 14, TechSearch must prove that the P6 microprocessors have both a native instruction width of N bits and an expanded RISC instruction comprised of M+N bits to be used when the computer is emulating, or their equivalents.

It is clear that none of the P6 microprocessors can possibly infringe the asserted claims, because it is beyond question that the P6 microprocessors do not have a "native mode" with microinstructions of N bits that is different from an emulation mode with microinstructions of M+N

bits. (Papworth Decl.[12] ¶¶ 20-22; Reines Corrected Decl. Ex. A, Flynn Rebuttal Rep. at 14-16.) All of the microinstructions that each of the P6 microprocessors process are always exactly the same width—73 bits.[13] (Papworth Decl. ¶ 21.) Regardless of the target instruction that they are processing, the microinstructions in the P6 microprocessors are always 73 bits.[14] (*Id.*; Reines Corrected Decl. Ex. A, Flynn Rebuttal Rep. at 16, citing 8250DOCOO221; 8203DOCOO172).) Unlike the '927 computer, the P6 always uses all bits. (*Id.* at 16.) The P6 products do not have a mode in which the computer only uses some of the bits and ignores others, as the '927 computer does. Thus, the P6 microprocessors do not have microinstructions with a native width of N bits at some times and microinstructions of M+N width at other times. The P6 products therefore lack these claim limitations in the patent, and no reasonable jury could find otherwise.

This difference is substantial, because the format of the user instructions that the P6 microprocessors use when executing an instruction from an "earlier version" of Intel's x86 instruction set are absolutely indistinguishable from the format of the user instructions that each of the P6 microprocessors uses when executing an instruction from the "current version" of the x86 instruction set. (Reines Corrected Decl. Ex. A, Flynn Rebuttal Rep. at 14-15.) Put simplistically, unlike the '927 invention, if you "take away" the instructions from the x86 instruction set, the P6 microprocessors cannot run. Even assuming that the P6 microprocessors emulate, namely, by emulating the instruc-

---

[12] David Papworth is Director of Microprocessor Development at Intel.

[13] In the more recent Pentium III microprocessor, the width is 77 bits.

[14] See n.11, *supra*.

tion sets of earlier versions of x86 instruction sets (Reines Corrected Decl. Ex. D, Hoevel Rep. at 4:25-27), the P6 products still do not infringe. The reason for this is the P6's do not emulate in the same way as the '927 patent, because the P6 runs only one instruction set. The way the P6 functions is substantially different from the emulation scheme required by the '927 patent.[15] Intel is, accordingly, entitled to summary judgment of noninfringement.

3.

There is an additional reason why the accused products do not infringe claims 4 and 14 of the patent, either literally or under the doctrine of equivalents.[16] Intel's P6 products do not have an "expanded instruction decoder[17] for using said M bits from each said expanded RISC instruction to redefine the RISC architecture computer in terms of the target computer" required by both claims, or its equivalent. ('927 patent at 53:50-54, 54:36-40.) To demonstrate

---

[15] While the patent does not require that emulation involve two different instruction sets (Claim Construction Order at 30), it should be noted that the P6's use of only one instruction set goes to whether the accused products, assuming that they emulate, do so in substantially the same way as the '927 invention.

[16] Claim 4 requires "an expanded instruction decoder for using said M bits from each said expanded RISC instruction to redefine the RISC architecture computer in terms of the target computer, wherein said M bits define fields. . . ." ('927 patent at 53:50-58.)

Claim 14 requires "an expanded instruction decoder for using said M bits from each said expanded RISC instruction to redefine the RISC architecture computer in terms of the target computer[.]" (*Id.* at 54:37-40)

[17] An "expanded instruction decoder" is not a type of decoder. The words "expanded instruction" simply describe what is decoded; they do not modify the word decoder.

infringement of these claim elements, TechSearch must prove that (1) the accused P6 microprocessors have an expanded instruction decoder or something insubstantially different, and (2) such an expanded instruction decoder uses M bits from each expanded RISC instruction to redefine the RISC architecture computer in terms of the target computer during emulation. It is, however, beyond cavil that the P6 products do not decode instructions as required by these claim elements either literally or under the doctrine of equivalents.

In its Claim Construction Order, the Court stated that the expanded instruction decoder is "[a] decoder that can decode expanded instructions." (Claim Construction Order at 32.) TechSearch does not claim that P6 microprocessors have such a decoder. Instead, TechSearch claims that an "alias multiplexer"[18] satisfies the decoder requirement. The multiplexer in the P6 microprocessors, however, differs materially from the decoder contemplated by the patent. (Papworth Decl. at 21; Reines Corrected Decl. Ex. A, Flynn Rebuttal Rep. at 29-30.)

All microcoded processors include a step that translates the instructions into a form that can be more directly processed by the arithmetic logic unit ("ALU"). This step in the patented invention involves considerable interaction between the various elements of the microinstruction. ('927 patent at, e.g., 53:50-58, 5:27-46.) The P6, on the other hand, uses a simpler scheme called "multiplexing" for this purpose, in which the inputs to the multiplexer are separately routed to the outputs, but do not otherwise interact with each other. Multiplexing is, thus, a simpler form of decoding, but the difference is substantial. Multiplexing is

---

[18] A multiplexer is "[a] device for funneling several different streams of data over a common communications line. . . ." Microsoft Computer Dictionary 302 (4th ed. 1999).

often used in standard microprocessors; the '927 patent decoding scheme, by contrast, is more complex. (*Id.*)

One of skill in the art knows that "decoders" and "multiplexers" perform substantially different functions, and are substantially structurally different. (Reines Corrected Decl. Ex. A, Flynn Rebuttal Rep. at 29-30.[19]) TechSearch's expert does not contend that the multiplexer in the P6 microprocessor is connected and operates as a decoder, or that it decodes anything in any way. However, "even accepting Dr. Hoevel's characterization of the operation of the P6 microprocessors, the function allegedly performed in the P6 microprocessors (*i.e.*, multiplexing) is not the same as the function required by the '927 patent claims (*i.e.*, decoding)." (*Id.* at 30:17-19.)

In addition, the structure of the multiplexer in the P6 microprocessor is "different from the structure of the decoder in the '927 patent which is a classic decoder physically divided" into a left-hand side and a right-hand side. (*Id.* at 30:22-23; *see also* '927 patent at figs 2&3, 5:27, 6:33-49. The decoder combines its input signals to produce outputs that cause selection of the direct, indirect or emulation registers needed for processing by the ALU. (*Id.* at 54:36-39, 44-49.) By contrast, the P6's "alias multiplexer" architecture does not combine its input signals, but simply steers each signal to the appropriate output field. (Papworth Decl.

---

[19] Indeed, the Microsoft Computer Dictionary (the same dictionary the Court relied upon at claim construction) defines the two terms as follows: Decoder is defined as "a type of circuit that produces one or more selected output signals based on the combination of input signals it receives," while a multiplexer is defined differently as "a device for funneling several different streams of data over a common communications line. . . ." Microsoft Computer Dictionary at 130, 302 (4th ed. 1999). The crucial difference between the two is that in a multiplexer, the data streams do not interact with one another.

¶¶ 14, 27.) Thus, even assuming that a multiplexer is a "subspecies" of decoder, the difference in structure and function is substantial. TechSearch attempts to create a triable issue of fact by arguing that a multiplexer is capable of acting as a decoder because it "produces one or more selected output signals based on the combination of input signals it receives." (TechSearch's Opp'n at 22:25-26.) TechSearch points to the Court's definition of "decoder" and states that the alias multiplexer produces "an output based on input signals that include 73-bit wide Cuops[20] and aliasable macroinstruction fields." (*Id.* at 20-21.) TechSearch does not, however, provide evidence to explain whether or how a multiplexer, which, unlike a decoder, by definition does not permit signals to combine, handles the *combination* of signals it receives similarly or equivalently to the expanded instruction decoder in the patent. Absent such evidence, TechSearch's assertion is not sufficient to generate a genuine issue of fact. (Greenspoon Decl. Ex. 5, Hoevel Decl. at 54.) Thus, Intel's evidence that the multiplexer, unlike a decoder, "does not produce one or more selected output signals based on the combination of input signals it receives" stands uncontradicted. (Papworth Decl. ¶ 27.) Dr. Hoevel's conclusory statements to the contrary fail to raise a genuine issue of material fact. (*See, e.g.*, Greenspoon Decl. Ex. 5, Hoevel Decl. ¶ 69.)

Finally, claims 4 and 14 require the instruction decoder to "redefine" the computer when emulating. ('927 patent at 53:51, 54:38.) No such redefinition takes place in the P6 microprocessors (Papworth Decl. at ¶ 22; Reines Corrected Decl. Ex. A, Flynn Rebuttal Rep. at 31.) Regardless of what x86 instruction is being executed, whether from an earlier

---

[20] The P6 architecture includes various forms of microcode. These are referred to as "microoperations" or "uops." As this microcode is processed by the multiplexer, it is converted from one form ("Cuops") to another ("Auops"). (Papworth Decl. ¶¶ 9-10.)

version of the x86 instruction set or not each of the P6 microprocessors processes microinstructions in exactly the same way. (*Id.*) Unlike the computer claims of 4 and 14 of the '927 patent, the P6 is simply not using an additional M bits to "redefine the computer" when it is supposedly emulating. Because the Cuops in the P6 microprocessors are always the same size (73 or 77 bits, depending on the microprocessor version), and all bits are required, there is no "redefinition" or "expansion" of these microinstructions when the computer is supposedly emulating. Regardless whether the x86 instruction being fetched at any given time is from an "earlier version," a current version, an MMX instruction, or any other x86 instruction, the Cuops are not "redefined" in any way, and no other reasonable jury could find otherwise. The P6 products therefore lack this limitation. ('927 patent at 53:51, 54:38.) This represents a substantial difference from the claims in the patent.

For these reasons, Intel's motion for summary judgment of noninfringement of claims 1, 4, and 14 of the '927 patent is granted.

4.

Having found Intel's P6 products do not infringe the independent claims of the '927 patent, one question remains: whether the dependent claims are also not infringed. Intel's motion for summary judgment relates to noninfringement of independent claims 1, 4, and 14, which are the only claims specifically mentioned in the complaint, and the Court only construed the independent claims at the *Markman* hearing. The complaint, however, accuses Intel of infringing "at least" claims 1, 4, and 14. The parties strongly disagree about whether TechSearch has placed the dependent claims at issue. This disagreement is of no moment because the determination that the independent claims of the patent are not infringed is tantamount to

finding that the corresponding dependent claims are not infringed. "One who does not infringe an independent claim cannot infringe a claim dependent on (and thus containing all the limitations of) that claim." *Wahpeton Canvas Co. v. Frontier, Inc.*, 870 F.2d 1546, 1552, n.9 (Fed.Cir. 1989) (citation omitted).[21]

Here, the dependent claims now asserted by TechSearch (namely, 2, 3, 5-13, & 15-25) are defined in terms of the independent claims, and contain all the limitations of the independent claims, as shown in the chart hereto annexed as Appendix A. The chart shows how each of the dependent claims asserted by TechSearch contains all of the elements of the independent claim associated with it. For this reason, Intel cannot infringe these dependent claims as a matter of law if the independent claims are not infringed.

III

For the reasons set forth above,

Accordingly,

**IT IS HEREBY ORDERED** that:

1. Intel's motion for summary judgment of noninfringement is GRANTED. Because the determination of noninfringement is dispositive, the Court does not reach the merits of the other motions for summary judgment relating to invalidity and enforceability, and dismisses them as moot.

2. Intel's *ex parte* motion to strike TechSearch's untimely submission of expert declarations that exceed the scope of its expert witness disclosures is DENIED as to Dr. Hoevel's declaration in opposition to summary judgment of nonin-

---

[21] Counsel for both parties agreed on this point at the hearing.

fringement. The Court does not reach the other declarations that Intel moves to strike because they are associated with the motions that the Court does not reach.

3. Intel's *ex parte* request for leave to file a reply re: Intel's *ex parte* motion to strike TechSearch's untimely submission of expert declarations that exceed the scope of its expert witness disclosures is DENIED.

4. Intel's counterclaim for declaratory relief is dismissed as moot.

5. This action is dismissed with prejudice.

Dated: January 31, 2000.

/s/ William H. Orrick
William H. Orrick
United States District Judge

## APPENDIX A

| Claim number: | Claim language: |
|---|---|
| 2. | A method for emulating the instruction set of a target computer on a RISC Architecture computer as in claim 1 . . . |
| 3. | The method of claim 2, wherein steps 1-9 occur during a time period comprised of . . .[steps 1-9 are listed in claim 1, with claim 2 adding additional matter to step 9]. . . |
| 5. | "The computer of claim 4, wherein [specifying memory location in relation to RISC architecture]. . . |
| 6. | "The computer of claim 4, wherein [specifying memory location in relation to RISC architecture] |
| 7. & 8. | "The computer of claim 6 . . . ." |
| 9. | "The computer of claim 4, wherein said target computer is [specifies target computer] . . . |
| 10. | "The computer of claim 4, where in said target computer is [specifies different target computer]. |
| 11. | The computer of claim 4, wherein said target computer is [specifies different target computer]. |
| 12. | The computer of claim 4, additionally comprising means . . . |
| 13. | "The computer of claim 4, wherein said instruction set is comprised of . . . additionally comprising means . . . |

| | |
|---|---|
| 15. | "The computer of claim 14, wherein said redefining means comprises using said M bits to define fields . . . . |
| 17. | "The computer of claim 14, [location of RISC architecture in relation to micro-code memory] . . . |
| 21. | The computer of claim 14, wherein said target computer is . . . . |
| 25. | "The computer of claim 14, wherein said instruction set is comprised of . . . additionally comprising means . . . . |

('927 patent at cols. 53-56.)

## APPENDIX G

[Filed December 16, 1999]

DO NOT PUBLISH OR INCLUDE IN DATABASE

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

| | | |
|---|---|---|
| TECHSEARCH L.L.C., | ) | Case No. C-98-3484 WHO |
| | ) | |
| Plaintiff, | ) | ORDER |
| vs. | ) | |
| | ) | |
| | ) | |
| INTEL CORPORATION, | ) | |
| | ) | |
| Defendant. | ) | |

Intel Corporation ("Intel") filed motions for summary judgment against plaintiff TechSearch, L.L.C. ("Tech Search"), claiming that the patent-in-suit is anticipated by prior art, that four of Intel's patents are prior art, that the patent-in-suit is not infringed, and that the patent is invalid. TechSearch filed cross-motions for summary judgment, claiming that the patent is enforceable and not anticipated. The Court having considered the pleadings, submissions on file and oral arguments of counsel,

IT IS HEREBY ORDERED that:

1. Intel's motion for summary judgment of non-infringement of the patent-in-suit is GRANTED.

2. Because the determination of non-infringement is dispositive, the Court does not reach the merits of the other above-mentioned motions for summary judgment.

3. The pretrial conference scheduled for January 11, 2000, and the trial scheduled for January 24, 2000, are hereby vacated.

4. A Memorandum Decision and Judgment will follow.

Dated: December 16, 1999.

/s/ William H. Orrick
William H. Orrick
United States District Judge

## APPENDIX H

[Filed November 15, 1999]

DO NOT PUBLISH OR INCLUDE IN DATABASE

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

| | | |
|---|---|---|
| TECHSEARCH L.L.C., | ) | Case No. C-98-3484 WHO |
| | ) | |
| Plaintiff, | ) | ORDER |
| vs. | ) | |
| | ) | |
| | ) | |
| INTEL CORPORATION, | ) | |
| | ) | |
| Defendant. | ) | |

Good cause appearing,

IT IS HEREBY ORDERED that:

1. On or before November 17, 1999, the parties shall furnish copies of all documents associated with briefing for the motions scheduled for hearing before this Court on November 23, 1999, and December 14, 1999, to the Court's Technical Advisor Dr. Anthony Hearn. The motions scheduled for hearing before the Court on the above dates are: Intel's motion for partial summary judgment regarding prior art under section 102(e), Intel's motion for summary judgment of invalidity, Intel's motion for summary judgment of non-infringement, Intel's motion for partial summary judgment of invalidity based on anticipation by the registration of the 3250 product description with the copyright office, Intel's motion for summary judgment of invalidity based on on-sale bar violation and best mode violation, TechSearch's motion for summary judgment of

enforceability, and TechSearch's motion for summary judgment that none of Intel's asserted prior art anticipates the independent claims of the patent-in-suit.

2. The copies should not be filed in the Clerk's Office or served upon opposing parties, but delivered to the Technical Advisor at RAND Corporation, 1700 Main Street, Santa Monica, CA 90401.

Dated: November 15, 1999.

/s/ William H. Orrick
William H. Orrick
United States District Judge

## APPENDIX I

WEIL, GOTSHAL & MANGES LLP
SILICON VALLEY OFFICE
2882 SAND HILL ROAD
SUITE 280
MENLO PARK, CA 94025-7022
(650) 926-6200
FAX: (650) 854-3713

DALLAS
HOUSTON
MIAMI
NEW YORK
WASHINGTON, D.C.

BRUSSELS
BUDAPEST
LONDON
PRAGUE
WARSAW

EDWARD R. REINES
DIRECT LINE
(650) 924-4222
EMAIL:
edward.reines@weil.com

August 1, 2000

**BY HAND DELIVERY**

Honorable William H. Orrick
United States District Court
Northern District of California
San Francisco Division
450 Golden Gate Avenue
San Francisco, California 94102

**Re: TechSearch LLP v. Intel Corporation**
***Civil Action No. C-98-03484 WHO***

Dear Judge Orrick:

We represent defendant Intel Corporation in this matter. As the Court will recall, the Court granted Intel's motion for summary judgment of noninfringement last winter. Defendant TechSearch's appeal of that ruling is now pending before the Court of Appeals for the Federal Circuit.

We write to suggest that the Court consider whether it makes sense to have Dr. Anthony Hearn (the Court's technical advisor in the above-referenced matter) sign an interim affidavit attesting that he has complied with the Court's appointment order for his work to date, instead of signing such an affidavit only at the "conclusion of his

appointment," as the Court originally ordered. *See* 11/9/99 Order at 7:1-3. At this point, no affidavit is due because the Court has not concluded Dr. Hearn's appointment. Indeed, Intel's inequitable conduct claim and fee request are still before this Court because this Court denied Intel's attorneys' fees request without prejudice to its right to renew that request after the appeal is resolved.

Nevertheless, we make this request because TechSearch has complained to the Federal Circuit about the Court's appointment of and use of Dr. Hearn. Specifically, although the Court's order is clear that Dr. Hearn need sign a compliance affidavit only upon the "conclusion of his appointment," TechSearch has asked the Federal Circuit to reverse the Court's summary judgment ruling because, among other reasons, Dr. Hearn has not yet signed a compliance affidavit. Based on the absence of a compliance affidavit in this record, TechSearch argues that Dr. Hearn improperly influenced the Court's decision, that he was largely unsupervised, that he systematically violated the Court's appointment order, and that he conduced "ex parte research discussions" and "secret experiments." TechSearch Appeal Brief (attached) at 10, 28; *see also id.* at 21 ("Perhaps in its haste to dispose of what it believed was a case involving technology too difficult to address in the conventional manner of other lawsuits, the district court let its expert, Dr. Hearn (and Special Master Thacher) take over.").

While we are confident that the Federal Circuit will understand the plain meaning of the Court's appointment order – that Dr. Hearn need sign a compliance affidavit later, only upon the "conclusion of his appointment" – we suggest that this Court may want to request Dr. Hearn to sign an interim compliance affidavit now, before Intel files its opposition brief on August 21, so the parties can avoid wasting more time and money on TechSearch's complaints.

If the Court chooses not to modify its order, however, we respect the Court's decision and look forward to Dr. Hearn signing a compliance affidavit at the conclusion of his appointment.

Respectfully submitted,

/s/ Edward R. Reines
Edward R. Reines

ERR:kac

Enclosure

cc: Anthony Hearn (w/enclosure)
Special Master Thacher (w/enclosure)
Raymond P. Niro, Esq. (w/o enclosure)

**APPENDIX J**

NIRO SCAVONE HALLER & NIRO
181 West Madison Street, Suite 4600
Chicago, Illinois 60602 - 4515

Telephone (312) 236-0733
Facsimile (312) 236-3137

August 2, 2000

**Facsimile Transmission—(415) 522-2184**

The Honorable William H. Orrick, Jr.
United States District Judge for the
Northern District of California
450 Golden Gate Avenue
San Francisco, California 94102

Re: TechSearch v. Intel; Case No. C 98-03484 WHO;
Appeal No. 00-1226

Dear Judge Orrick:

This concerns Mr. Reines' letter of August 1, 2000 regarding Intel. TechSearch opposes the relief sought by Intel.

A district court no longer has jurisdiction once an appeal has been taken. The notice of appeal in this case was filed on February 8, 2000. TechSearch's appeal was stayed pending the Court's resolution of Intel's Rule 59 and Rule 60 motions. Those motions were denied on May 12, 2000. The Federal Circuit then reactivated TechSearch's appeal. On May 19, Intel itself filed an amended notice of cross appeal. This case is on appeal and is subject to the jurisdiction of the Court of Appeals for the Federal Circuit. Intel has

failed to point to any jurisdictional basis for the action it now asks this Court to take.

Intel is also extremely tardy. It has known since the grant of summary judgment in this case on December 16, 1999 that Dr. Hearn did not provide an affidavit upon completion of his employment as required by the last unnumbered paragraph on page 7 of the Court's Memorandum Decision and Order of November 9, 1999. If Intel was not aware of the shortcoming at that time, it was most certainly aware of it at the time Dr. Hearn submitted his statement, which was attached to the Court's Order dated February 3, 2000. It was abundantly clear that Dr. Hearn's employment was completed by November 30, 1999 (see Exhibit A to the February 3 Order) and certainly no later than the date of the Court's Order requiring payment to Dr. Hearn.

Nevertheless, Intel let this matter slide until its letter of July August 1, 2000, long after it knew TechSearch's brief would be due. In fact, TechSearch's brief was served upon Intel's counsel on July 12, 2000. To allow Intel to now modify the record *post hoc* to enhance its chances on appeal would be unfairly prejudicial to TechSearch, even if there were a jurisdictional basis.

TechSearch therefore respectfully requests that the relief sought by Intel be denied.

Sincerely,

/s/ Joseph N. Hosteny
Joseph N. Hosteny

JNH:bz
cc: Special Master James F. Thacher (415-989-7319)
Edward Reines, Esq. (650-854-3713)
Dr. Anthony Hearn (310-393-4818)
Tyree Jones (707-220-4704)